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LOAD PROGRAMMER, STATIC SWITCHES, AND ANNUNCIATOR FOR INVERTERS AND CONVERTERS

by

R. W. BRIGGS, C. L. DOUGHMAN, R. D. JESSEE,
AND E. F. SWIDERSKI

prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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Westinghouse Electric Corporation
AEROSPACE ELECTRICAL DIVISION
LIMA, OHIO

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TOPICAL REPORT

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PREFACE

Technical Manager of this program for the NASA Lewis Research Center was Mr. Francis Gourash.

The entire program "Parallel Operation of Static Inverters and Converters and Evaluation for Magnetic Materials" is reported in four topical reports and a summary report.

"Inverter-Converter Parallel Operation" (ref. 1) defines and experimentally verifies the circuit conditions that must exist for operating static inverters and static converters in parallel.

"Inverter-Converter Automatic Paralleling and Protection" (ref. 2) defines and experimentally verifies the electrical control and protection circuits necessary for isolating faulted inverters and converters from a parallel system while maintaining continuity of high-quality electric power to load equipment.

"Evaluation of Magnetic Materials for Static Inverters and Converters" (ref. 3) defines the magnetic characteristics of improved materials for magnetic components as applied in advanced static inverters or static converters.

"Load Programmer, Static Switches and Annunciator for Inverters and Converters" assesses the characteristics of static electrical switches for both ac and dc systems; defines the characteristics of a load programmer for maintaining power to the critical system loads, and provides an annunciator function for displaying inverter and/or converter operating conditions.

"Parallel Operation of Static Inverters and Converters and Evaluation of Magnetic Materials" (ref. 4) summarizes the four topical reports.

LOAD PROGRAMMER, STATIC SWITCHES, AND ANNUNCIATOR FOR INVERTERS AND CONVERTERS

By R. W. Briggs, C. L. Doughman, R. D. Jessee, and E. F. Swiderski

ABSTRACT

A load programmer concept developed for an electric power system compares system capacity to load demand and, as required, automatically removes lower-priority loads.

Characteristics and experimental test results of a three-phase static switch and a dc switch are analyzed. Circuit interruption times of less than three milliseconds are obtained for current loads up to 250 percent of rated value.

An annunciator developed to operate in conjunction with the control and protection circuits visually displays the state of either a dc or an ac system consisting of multiple paralleled converters or inverters.

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LOAD PROGRAMMER, STATIC SWITCHES, AND ANNUNCIATOR FOR INVERTERS AND CONVERTERS

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SUMMARY

A concept is developed for a load programmer to be used in a three-phase, paralleled, alternating-current electrical system using static inverters. The programmer automatically determines whether the electrical loads exceed the system capacity. If the system capacity is exceeded, low-priority loads are automatically removed. If system capacity is not exceeded, conditions are established which permit additional loads to be applied.

The characteristics of a three-phase static switch rated at 2.2 amperes and 115 volts per phase are analyzed, and test results are obtained from an experimental model. Circuit interruption times of approximately one millisecond are obtained for current loads up to 250 percent of rated value.

Similar circuit analyses and test results on an experimental model are discussed for a static, direct-current switch rated at 40 amperes and 150 volts. Circuit interruption times are approximately one millisecond for rated load and increase to 2-3 milliseconds for 250 percent load current.

An annunciator system developed to operate in conjunction with the control and protection circuits visually display the state of either a dc system or an ac system consisting of multiple converters or inverters, respectively, operating in a parallel or an isolated mode. Two experimental models were built to operate with the inverter/converter systems described in the report entitled "Inverter-Converter Automatic Paralleling and Protection" (ref.2).

SYMBOLS

ICC	Inverter Control Contactor
CCC	Converter Control Contactor
LBC	Load Bus Contactor
TBC	Tie Bus Contactor

LCC	Load Control Contactor
MOS	Manual Override Switch (Resets Subsystem)

The following nomenclature is used exclusively in the load programmer portion of this report.

LBA	Line Breaker A
LBB	Line Breaker B
TBA	Tie Breaker A
TBB	Tie Breaker B
OLi	Overload Logic Signal for Removing Priority i Load Groups by Tripping Load-Group Switches
GOi	Load Capacity Logic Signal for Adding Priority i Loads by Closing Load-Group Switch
I_i	Actual Current Magnitude to Priority i Loads
I_{iP}	Anticipated Current to Priority i Loads
iA_j	Load Group of Priority i Connected to Subsystem A
iB_j	Load Group of Priority i Connected to Subsystem B
i	Priority Number Associated with a Load Group
j	The jth Switched Load of a Priority Load Group

INTRODUCTION

As space missions become more complex and increase in scope and duration, the required magnitude of electric power will increase. One approach for achieving this larger amount of electric power is to use multiple static inverters or static converters and to operate these inverters or converters in parallel. While parallel system operation may be necessary to deliver sufficient power to certain electrical loads, provisions should be included in the system so that the inverters or converters can independently supply individual load busses. This isolated operation also provides the ability for isolating various segments of the electrical system should a failure or malfunction occur.

This concept of parallel system operation has been utilized in military and commercial aircraft for several years. These aircraft applications have used rotating ac generators as the primary source of electric power.

In contrast to aircraft systems, the system concept used as a basis for this program consists of all static equipment and assumes that the primary source of electric power on the space vehicle is direct current which, for example, could be a solar cell array or a solar cell array and battery combination.

Figure 1 presents a line diagram for an electric power system which might be used in a space vehicle. This line diagram consists of a dc bus which is the main source of electric power. For an ac system, a static inverter is connected to this dc bus through an electrical contactor. The inverter output power is then delivered to a load bus for utilization. The inverter output is also connected, by contactors, to a tie bus which permits parallel operation of multiple inverters.

Should the electrical loads require dc power at a voltage level higher than the dc bus, static converters are used in place of the static inverters.

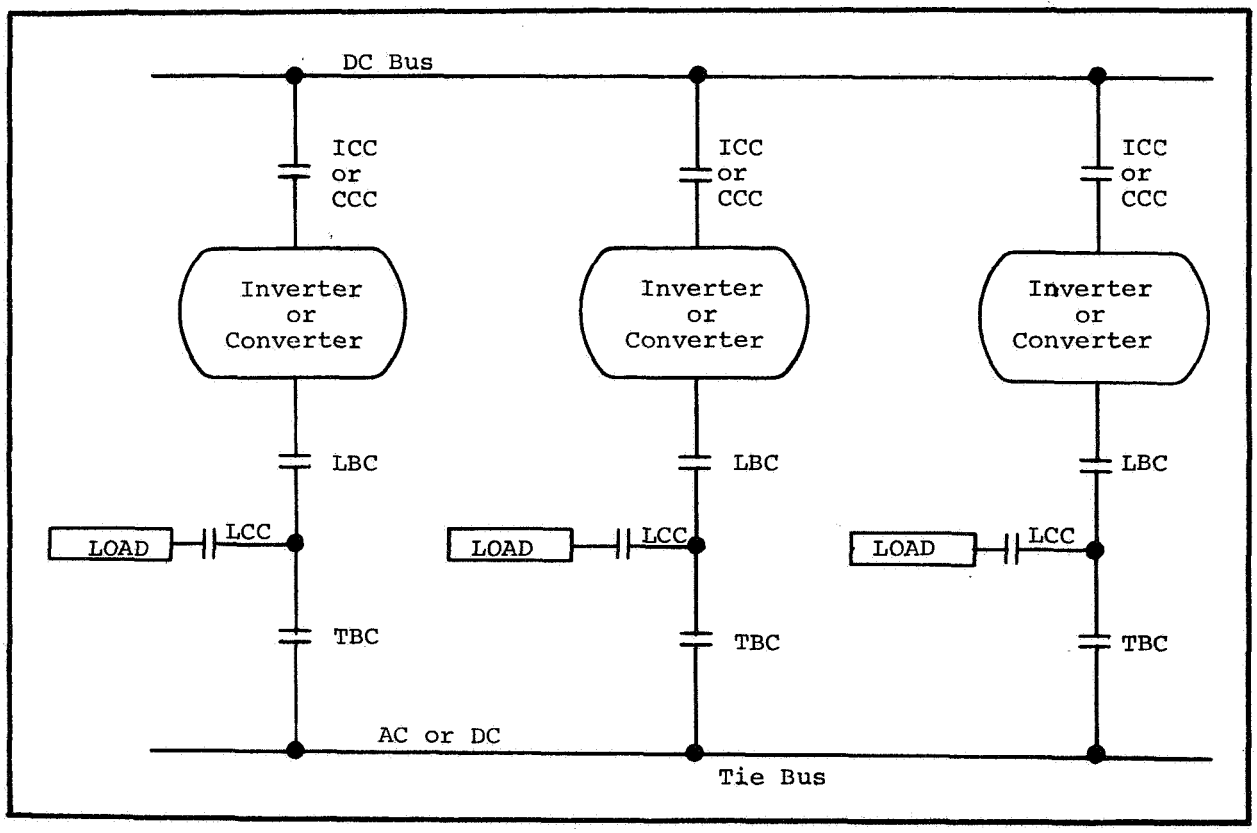


Figure 1. - Electric Power System Configuration

A space vehicle has a limited electric power capacity and also has certain electrical loads that are the most critical (e.g., life support). Therefore, one wants to supply power to these most critical loads to the maximum extent. Should the power system capacity be reduced because of a malfunction or failure, lower priority loads need to be removed to maintain continuous power to the highest-priority loads. One method for selectively delivering power to various priority loads is to use a load programmer within the system. Such a programmer has been studied as presented herein.

As shown in figure 1, electrical contactors are necessary to achieve parallel system operation and to provide means for isolating various segments of the electrical system. In previous aircraft electrical systems, these contactors have been electromagnetic devices which have certain inherent limitations because of their moving mechanical contacts. These limitations include susceptibility to contact contamination and pitting from hostile environments. Severe design criteria of mechanical shock and vibration, vacuum operation, fast response, repeated cycling, minimum contact bounce, longlife, and high reliability are difficult to attain with electromechanical contactors.

The silicon semiconductor devices, with associated circuits for controlling switching, make it possible to duplicate the electromagnetic contactor action without the use of moving parts. Therefore, the use of silicon semiconductor devices as static switches can eliminate some of the principal disadvantages of electromechanical contactors, especially for space vehicle applications.

Both ac and dc static switches were developed and evaluation tests were performed on experimental models.

It is sometimes necessary to portray the condition, or state, of an electrical system such as shown in figure 1. For example, an astronaut or operator on a space vehicle needs to know whether contactors are open or closed, whether a malfunction has occurred and if so what constitutes the malfunction and where it is located. This type of information can be obtained electrically and can be displayed by an annunciator. An experimental annunciator for use with inverter/converter systems as described in the report entitled "Inverter-Converter Automatic Paralleling and Protection" (ref. 2) was developed.

These three elements (load programmer, static switches, and annunciator) will probably be required in future manned space vehicles of long-mission duration.

LOAD PROGRAMMER

Purpose of Study

The purpose of the load programmer study was to determine the requirements for a general-type load programmer. While the load programmer can be adapted to various load profiles or various priority levels, this analysis is based on four load priorities to provide an analytical base for the techniques presented. Although the analysis presented discusses the inverter system in particular, the derived equations and basic approach also apply to converter systems. The primary difference lies in the current and voltage sensing circuits. The programmer functions considered in the analysis are:

1) Monitor total system and subsystem loads to provide full utilization of the available power system capacity.

2) Establish a load priority, applicable to various load profiles, to maintain a continuous flow of power in accordance with the selected load priority despite faults or conditions that would otherwise overload the system.

Load Priorities

Loads of four priorities are to be supplied power from an electric power system of three-phase inverters that normally operate in parallel through a tie bus. A load bus is connected to each inverter, such that loads may be supplied by either the parallel system or by a single inverter. Load priorities are assumed to be as follows:

1) Loads of priority #1 are essential loads, without which a mission would have to be abandoned immediately. Such loads would probably be redundant. The loads are assumed to be continuous.

2) Loads of priority #2 are essential for completion of a mission. Temporary loss of priority #2 loads, however, will not require abandonment of a mission.

3) Loads of priority #3 are necessary for the fulfillment of all planned activities of a mission. These loads do not demand a rigorous schedule. Loss of these loads will require a reduction of activities and may shorten the useful mission time.

4) Loads of priority #4 are convenience loads and may be used only when power capacity permits. Loss of these loads will not jeopardize a mission in any way but may reduce the comfort or convenience level.

Basic Concepts

Electric power system functions and protection. - The basic function of the electric power system is to supply power continuously to all the load busses. A conventional power distribution system is illustrated in figure 1. If any inverter loses its capacity to supply power to the parallel system, it must be isolated from the paralleled system. If such inverter can supply power in an isolated mode, its load bus is removed from the parallel system and is supplied by the isolated inverter. If however, the inverter cannot supply power of the required quality, the load bus is connected to the parallel system tie bus and the inverter is removed from service.

Loss of inverter capacity may be the result of a failure within the inverter, of a fault in feeder lines associated with the inverter, or of a failure of the dc power supply. Faults which cause the loss of inverter capacity should cause immediate isolation and shutdown of the inverter without opening the tie bus where possible. Certain faults (such as a tie bus or load division fault) can cause the loss of the capability of parallel operation of an inverter, but not necessarily its capacity to supply acceptable quality power. In case of such faults, isolated operation is indicated. The quality of power which is acceptable is a function of the connected loads. Many loads can operate successfully from sources having a good deal of degradation of quality, while a few cannot. The decision as to whether or not to remove an inverter from service is thus dependent upon the relative importance of power quality versus system capacity. This decision could be a function of a load programmer, but such a function has not been considered in this study.

It is assumed in this study that the control and protection system will automatically take the required action under fault and overload conditions so as to make power available at each load bus except when a fault exists on the load bus. Should a fault occur on the load bus, loads connected to that bus are out of service and require maintenance to restore them to service. It is further assumed that faults occurring on the loads themselves will be cleared within the distribution system by proper fusing or local circuit breaker action. An inverter overload occurs only when one or more inverters are individually overloaded. In other words, loading a particular bus to a current greater than the rating of a single inverter does not constitute an overload unless the current drawn from one inverter exceeds its rating.

Functions of the load programmer. - The load programmer is a control system which operates in conjunction with the electric power system to automatically switch load centers on or off depending on the load priority, load demand and system capacity. The

relative magnitude of each of the four priorities of load is unknown, and the total installed load may exceed the capacity of the electric power system.

In this concept of the load programmer, it is assumed that the load busses (one for each inverter) are as reliable as is any point where loads may be connected. The priority #1 loads are, therefore, connected directly to the load busses and are distributed more or less equally among available load busses. Redundant loads are connected to separate load busses. Controls for switching to standby redundant loads are considered as part of the loads. No provision is made in the load programmer, therefore, to switch off priority #1 loads.

Loads of lower priorities may, likewise, be distributed among the load busses. While distribution affects the number of control elements necessary in the load programmer, the concept of the programmer itself is not affected. So long as all inverters operate in parallel, a single load center for a single priority is sufficient, relative to the load programmer. If only low priority loads, however, are connected to a particular load bus, its inverter is lost to higher priority loads if that inverter cannot operate in parallel. It is, therefore, assumed that loads of all priorities will be distributed among all load busses.

The load programmer allows loads of any priority to be added by an operator or by automatic means so long as the system capacity is not exceeded. Should the addition of load cause the system capacity to be exceeded, an overload signal initiates the removal of lower priority loads, starting with those of lowest priority. Likewise, the removal of higher priority loads increases the available capacity and thus may automatically reconnect load centers of lower priority to the system. Also, the loss of an inverter, which reduces the system capacity, causes lower priority loads to be dropped so that available capacity is not exceeded.

When one or more inverters operate isolated from the parallel system, the load programmer operates as two separate control systems. One control system deals with the parallel system, and the other with the isolated system independently, although the same rules apply to both. Load priorities of the isolated system are, therefore, independent of the parallel system. It is possible to observe priority ratings throughout the entire power system, where isolated operation occurs, only by adding considerable complication in form of controls and load transfer switches. Since isolated inverter operation is an abnormal mode of operation, in the interest of simplicity isolated inverters are considered as independent systems. This concept, of course, is a deviation from the strict priority concept. For example, an isolated inverter could supply power to priority #4 loads even though priority #3 loads have been removed from the parallel system.

The load programmer, therefore, allows full utilization of the available capacity of the power system, while preventing overloading even though the installed load may greatly exceed the power system capacity.

Implementation of Load Programmer

In the following discussion, it is intended to set up guidelines for the design of a load programmer which functions as described in the foregoing discussion. Although the circuits shown can be used in design of the load programmer, they are exemplary in nature, and not restrictive. Equations employed are necessarily general. Design of a load programmer requires specific information and is, therefore, beyond the scope of the present study.

Consider load busses A and B, shown in figure 2, as possible load arrangements, where each load bus is powered by a separate inverter and is connected to the system tie bus. Loads are identified along with their associated switches according to priority and circuit identity. Each load shown in the figure represents a group

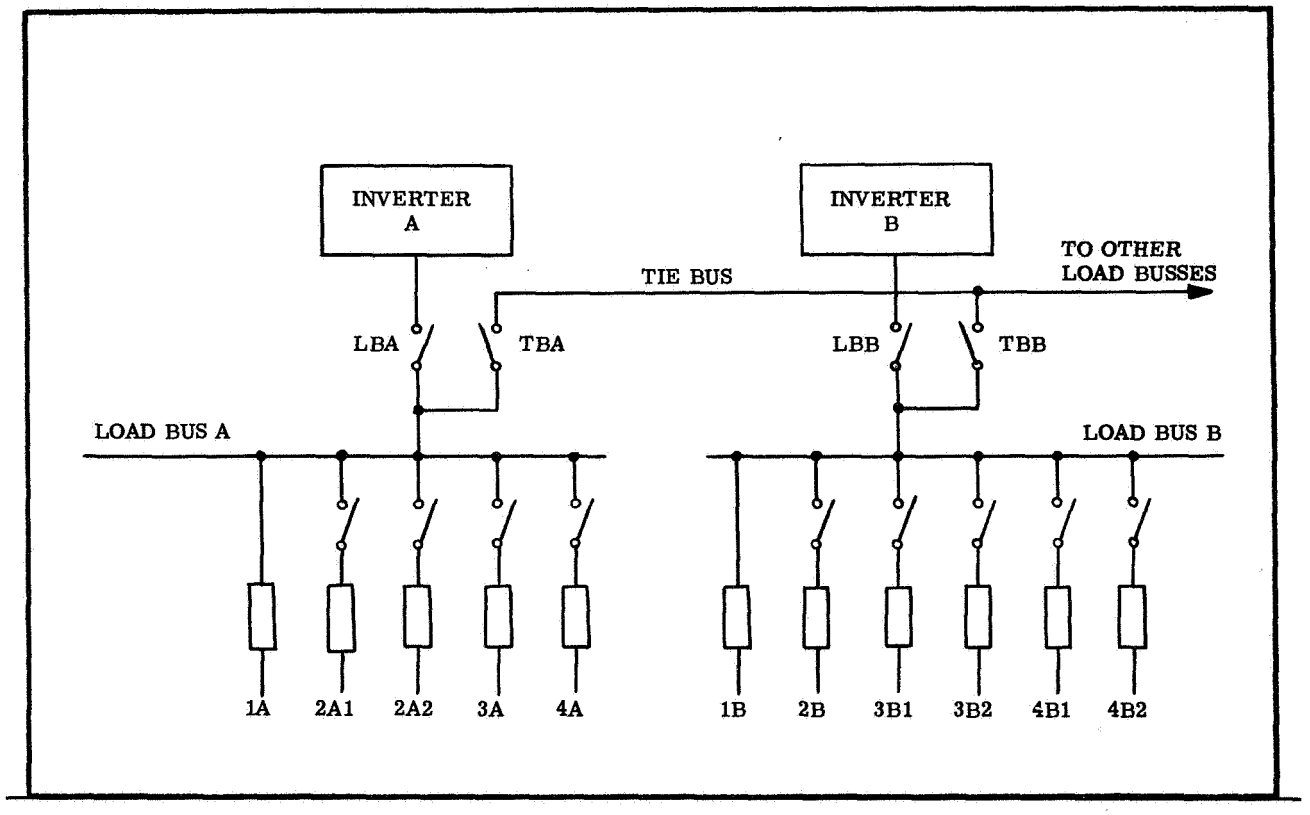


Figure 2. - Simplified Block Diagram of Load Circuits

of loads which may include a distribution network, circuit breakers, switches, etc. In a given priority, each group represents an arbitrary unit of load. Load circuits shown with the same priority, therefore, draw approximately equal currents when fully on. Load groups of different priorities, however, do not necessarily draw equal currents. The load-group switches of figure 2 are considered as relays responsive to logic signals and having auxiliary contacts usable to detect the state of the switch (closed or tripped). Each load-group switch is individually responsive to appropriate logic signals.

Load switching. - There are two reasons for removing a load: (1) the operator or automatic control commands it or (2) load exceeds capacity. Likewise, reasons for adding load are: (1) operator or automatic command or (2) capacity becomes available when prior command exists.

Let the operator command signals be identified by the load circuit identification. For example, 2A1, 2A2, 3A, etc., are command signals to close load-group circuits 2A1, 2A2, 3A, etc., while $\overline{2A1}$ (not 2A1), $\overline{2A2}$, $\overline{3A}$, etc., are trip signals.

If the maximum rated current of one inverter is I_m, then an overload will occur in the parallel system when $I_L/N > I_m$, where I_L is the total system load current and N is the number of inverters operating in parallel. When an overload occurs, a logic signal is produced for each inverter, designated as OLi.

Arbitrary addition of loads to the power system may cause overloads. A function of the load programmer is that of anticipating not only the approximate magnitude of a load to be added but also its priority. If a command to add load is given, the load will be accepted if sufficient capacity is available or if lower priority loads, when removed, make sufficient capacity available. An overload signal may, therefore, be initiated by a command to add high priority load.

To develop the necessary anticipatory signals, the load-group switches must be monitored along with their command signals. Any time that a command signal exists and the load-group switch is open, a signal is received which anticipates the current that will be drawn once the switch closes. Having closed, however, the switch removes this signal.

Let the anticipated current be designated as I_{ip} where specific identification replaces i in the subscript. The magnitude of I_{ip} is dependent on the number of unsatisfied command signals.

Actual currents must also be monitored according to load priority. These currents are designated, in decreasing priority, as I_1, I_2, I_3, and I_4.

Load removal logic: A current-dependent logic signal is required for each independent load-switching function. Considering first a parallel system only, three signals are needed for load removal.

$$OL4 = 1 \text{ if } (I_1 + I_2 + I_3 + I_4 + I_{2P} + I_{3P} > NI_m)$$

$$OL3 = 1 \text{ if } (I_1 + I_2 + I_3 + I_{2P} > NI_m)$$

$$OL2 = 1 \text{ if } (I_1 + I_2 > NI_m)$$

These signals represent overload conditions (either actual or anticipated) and are sufficient to remove loads of appropriate priorities. Trip signals for load-group switches with their output signals are as follows.

Logic Signal	Output
TRIP 4A = OL4 + $\overline{4A}$	T4A
TRIP 4B1 = OL4 + $\overline{4B1}$	T4B1
TRIP 4B2 = OL4 + $\overline{4B2}$	T4B2
TRIP 4C = OL4 + $\overline{4C}$	T4C
etc.	etc.
TRIP 3A = OL3 + $\overline{3A}$	T3A
TRIP 3B1 = OL3 + $\overline{3B1}$	T3B1
TRIP 3B2 = OL3 + $\overline{3B2}$	T3B2
etc.	etc.
TRIP 2A1 = OL2 + $\overline{2A1}$	T2A1
TRIP 2A2 = OL2 + 2A2	T2A2
TRIP 2B = OL2 + $\overline{2B}$	T2B
etc.	etc.

In the previous logic equations, each switch receives a trip signal from either the current signal or from local command.

Load addition logic: As in the case of load removal, three current signals are needed to add load of three priorities to a parallel system.

$$GO2 = 1 \text{ if } (I_1 + I_2 + I_{2P} < NI_m)$$

$$GO3 = 1 \text{ if } (I_1 + I_2 + I_3 + I_{2P} + I_{3P} < NI_m)$$

$$GO4 = 1 \text{ if } (I_1 + I_2 + I_3 + I_4 + I_{2P} + I_{3P} + I_{4P} < NI_m)$$

These signals indicate that a given priority of load is acceptable to the system. Close signals for load-group switches are as follows:

$$\begin{aligned} \text{CLOSE } 2A1 &= GO2 \cdot 2A1 \\ \text{CLOSE } 2A2 &= GO2 \cdot 2A2 \\ \text{CLOSE } 2B &= GO2 \cdot 2B \\ &\text{etc.} \end{aligned}$$

$$\begin{aligned} \text{CLOSE } 3A &= GO3 \cdot 3A \\ \text{CLOSE } 3B1 &= GO3 \cdot 3B1 \\ \text{CLOSE } 3B2 &= GO3 \cdot 3B2 \\ &\text{etc.} \end{aligned}$$

$$\begin{aligned} \text{CLOSE } 4A &= GO4 \cdot 4A \\ \text{CLOSE } 4B1 &= GO4 \cdot 4B1 \\ \text{CLOSE } 4B2 &= GO4 \cdot 4B2 \\ &\text{etc.} \end{aligned}$$

Isolated operation. - Consider now an inverter and loads isolated from the parallel system. The removal and addition of loads follow the same logic as does the parallel system. The currents to be sensed, however, are those which flow from the isolated load bus rather than the sum of load currents. A set of logic signals must, therefore, be developed for each load bus and must apply to only its own loads. The signals are duplicates in form to those of the parallel system. For inverter and load bus A, for example, the equations for logic are:

$$OL4A = 1 \text{ if } (I_{1A} + I_{2A} + I_{3A} + I_{4A} + I_{2AP} + I_{3AP} > I_m)$$

$$OL3A = 1 \text{ if } (I_{1A} + I_{2A} + I_{3A} + I_{2AP} > I_m)$$

$$OL2A = 1 \text{ if } (I_{1A} + I_{2A} > I_m)$$

The load removal signals similarly are

$$TRIP\ 4A = OL4A + \overline{4A}$$

etc.

The add signals are similar

$$GO2A = 1 \text{ if } (I_{1A} + I_{2A} + I_{2AP} < I_m)$$

etc.

$$CLOSE\ 2A1 = GO2A \cdot 2A1$$

etc.

Sensing circuits. - Figure 3 is a line diagram of a parallel inverter system showing two of the channels. Included are the current sensing circuits and the load bus arrangements. Loads are assumed the same as in figure 2.

In parallel operation the line breakers, LBA, LBB, etc., and the tie breakers, TBA, TBB, etc., are in the closed position, along with their auxiliary contacts. The current transformers are thus connected in parallel groups, with each transformer loaded by a burden, R. So connected, the output voltage of each group is proportional to the sum of the primary current. Voltage v_4 is, therefore, a measure of the total system current, v_3 is a measure of the total system current less that drawn by priority #4 loads, etc.

Loss of an inverter from the parallel system removes the resistor from each current transformer of the affected channel. This increases the burden on the parallel transformer group and increases the signal voltages v_4, v_3, and v_2, indicating that the system capacity has been reduced.

If a tie breaker is opened, leaving an inverter operating isolated, the current transformers of the affected channel, with their burdens, are isolated from the parallel group. The output signal voltage, v_{4A} for example, is proportional to the current in the isolated loads and not affected by the parallel system. Removal of the current transformer burden with the isolated channel increases the sensitivity to load current of the signal voltages v_4, v_3, and v_2, reflecting the reduced parallel system capacity.

Current sensing equations for a parallel system: In figure 3

$$v_2 = k(I_1 + I_2)R/N \tag{1}$$

$$v_3 = k(I_1 + I_2 + I_3)R/N \tag{2}$$

$$v_4 = k(I_1 + I_2 + I_3 + I_4)R/N \tag{3}$$

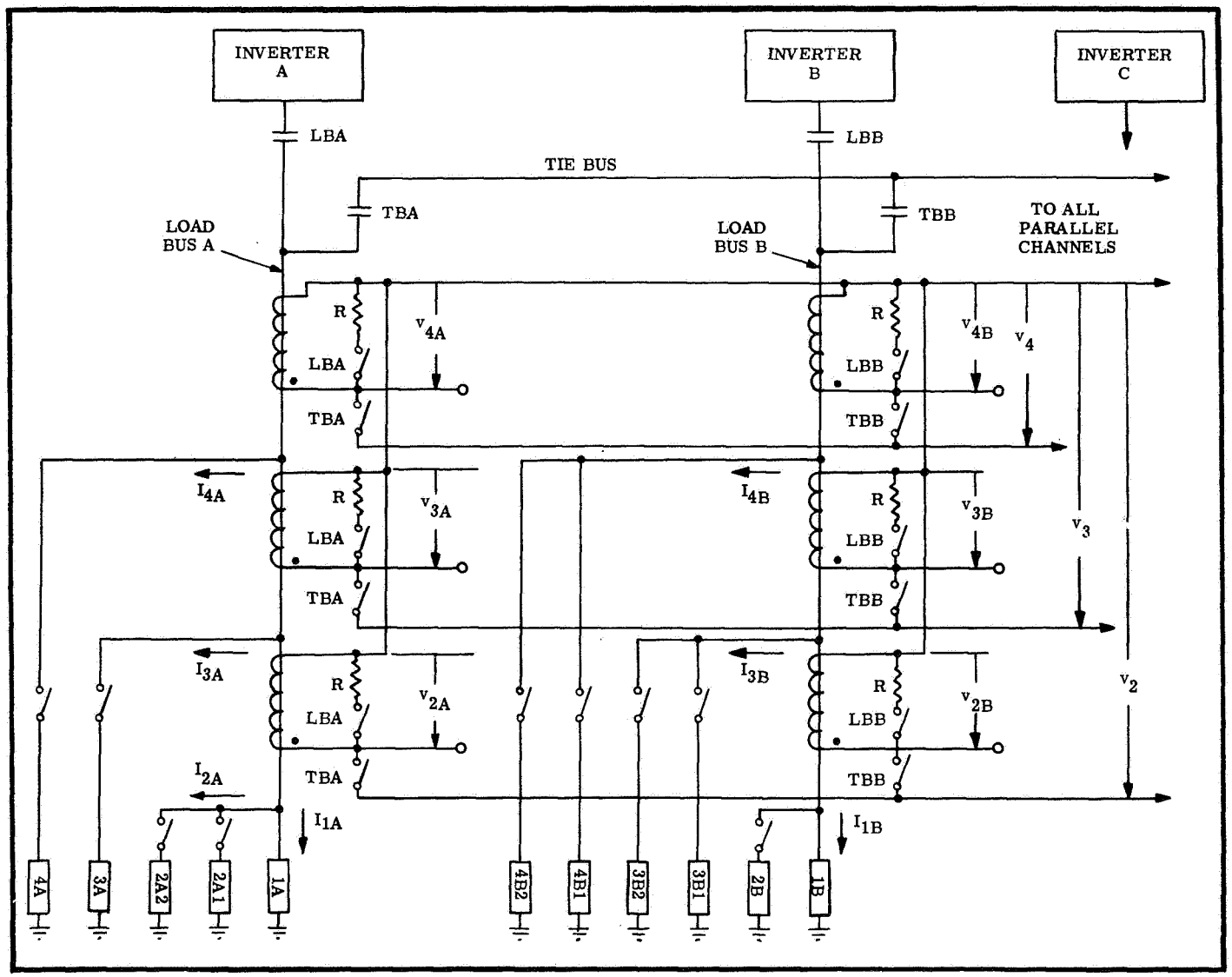


Figure 3. - Line Diagram of Current Sensing Circuits in Paralleled Inverter System

where

$$I_1 = I_{1A} + I_{1B} + I_{1C} + \ldots.$$

$$I_2 = I_{2A} + I_{2B} + I_{2C} + \ldots.$$

etc.

R = Resistance of current transformer burden.
N = Number of inverters operating in parallel.

Current sensing equation for an isolated system:

$$v_{2A} = k(I_{1A} + I_{2A})R \tag{4}$$

$$v_{3A} = k(I_{1A} + I_{2A} + I_{3A})R \tag{5}$$

$$v_{4A} = k(I_{1A} + I_{2A} + I_{3A} + I_{4A})R \tag{6}$$

etc. for each channel

Load anticipation circuits: Inasmuch as the load-current sensing signals are voltages (figure 3), the anticipated load signals must also be voltages of the proper magnitude, such that they may be added to give the desired monitoring signals.

Consider the required add-load signal, GO2, which exists only when

$$I_1 + I_2 + I_{2P} < NI_m, \tag{7}$$

or

$$\frac{I_1 + I_2}{N} + \frac{I_{2P}}{N} < I_m. \tag{8}$$

A circuit for detecting the current relation of equation (8), can be synthesized by substituting the voltage equation

$$v_2 + v_{2P} < v_m, \tag{9}$$

where

$$v_2 = kR\,\frac{(I_1 + I_2)}{N} \tag{10}$$

$$v_m = K_m I_m, \tag{11}$$

$$v_{2P} = k_2 V_{n_2}/N \tag{12}$$

In the above equations v_m is a voltage proportional to the maximum rated current of one inverter (I_m) and k, k_m and k_2 are constants of proportionality. V is the tie bus voltage and n_2 is the number of load-group switches in the parallel system in the tripped position but having close command signals. The constants may be related by substituting equations (10), (11), and (12) into equation (9).

$$kR \frac{(I_1 + I_2)}{N} + \frac{k_2 V_{n2}}{N} < k_m I_m \tag{13}$$

Comparing equation (13) with equation (8)

$$k_m = kR \tag{14}$$

and

$$k_2 V_{n_2} = I_{2P} \tag{15}$$

or

$$I_{2P/n_2} = k_2 V \tag{16}$$

The value of I_{2P/n_2} is the anticipated current per load group for priority #2 loads.

Similarly, for priority #3 loads,

$$v_3 + v_{3P} < v_m \tag{17}$$

$$v_3 = kR(I_1 + I_2 + I_3)/N \tag{2}$$

$$v_{3P} = k_3 V_{n_3}/N \tag{18}$$

$$k_3 V = I_{3P}/n_3 \tag{19}$$

and for priority #4 loads

$$v_4 = v_{4P} > v_m \tag{20}$$

$$v_4 = kR(I_1 + I_2 + I_3 + I_4)/N \quad (3)$$

$$v_{4P} = k_4 V_{n4}/N \quad (21)$$

$$k_4 V = I_{4P}/n_4 \quad (22)$$

Anticipated current detection circuits: A circuit for obtaining a voltage signal proportional to anticipated load is shown in figure 4, consisting of voltage transformers and switches. The number of voltage transformers is equal to the number of inverters operating in the system. The primary windings of these transformers are connected in series between the tie bus and ground. The secondary windings are connected through auxiliary contacts of the line breakers and the tie breakers. If both breakers of an inverter are closed so that the inverter is connected to the tie bus, the transformer secondary is connected to a common output point; otherwise, the secondary is short circuited to ground. The result is that the transformer secondary windings of only the parallel units are connected in parallel while the others are grounded. The tie-bus voltage, V, is thus distributed equally across the transformer primary windings of the parallel units because all other transformers are short circuited and will not support a voltage. The output voltage, V/N, is therefore, inversely proportional to the number of transformers connected in parallel. The turns ratio is assumed to be unity. (Note that if all transformers are short circuited, it is because the tie bus is isolated; hence no voltage is applied.)

The second group of transformers is associated with the load-group switches. One transformer is used with each load group. Each transformer is connected through a switch (L2A, etc.) which closes when a group-switch command signal is present and the group switch is tripped. The transformer primary winding is thus connected to either the voltage source, V/N, or to ground through the appropriate tie breaker auxiliary switch (TBA, etc.). The secondary windings associated with a particular load priority are connected in series such that the sum of their output voltages is a function of, n_i, the number of transformers connected to the voltage source V/N. (All switches (L2A, etc.) not closed, short circuit the primary windings.)

The output voltages of the circuit are thus

$$V_{2P} = k_2 n_2 (V/N)$$

$$V_{3P} = k_3 n_3 (V/N)$$

$$V_{4P} = k_4 n_4 (V/N)$$

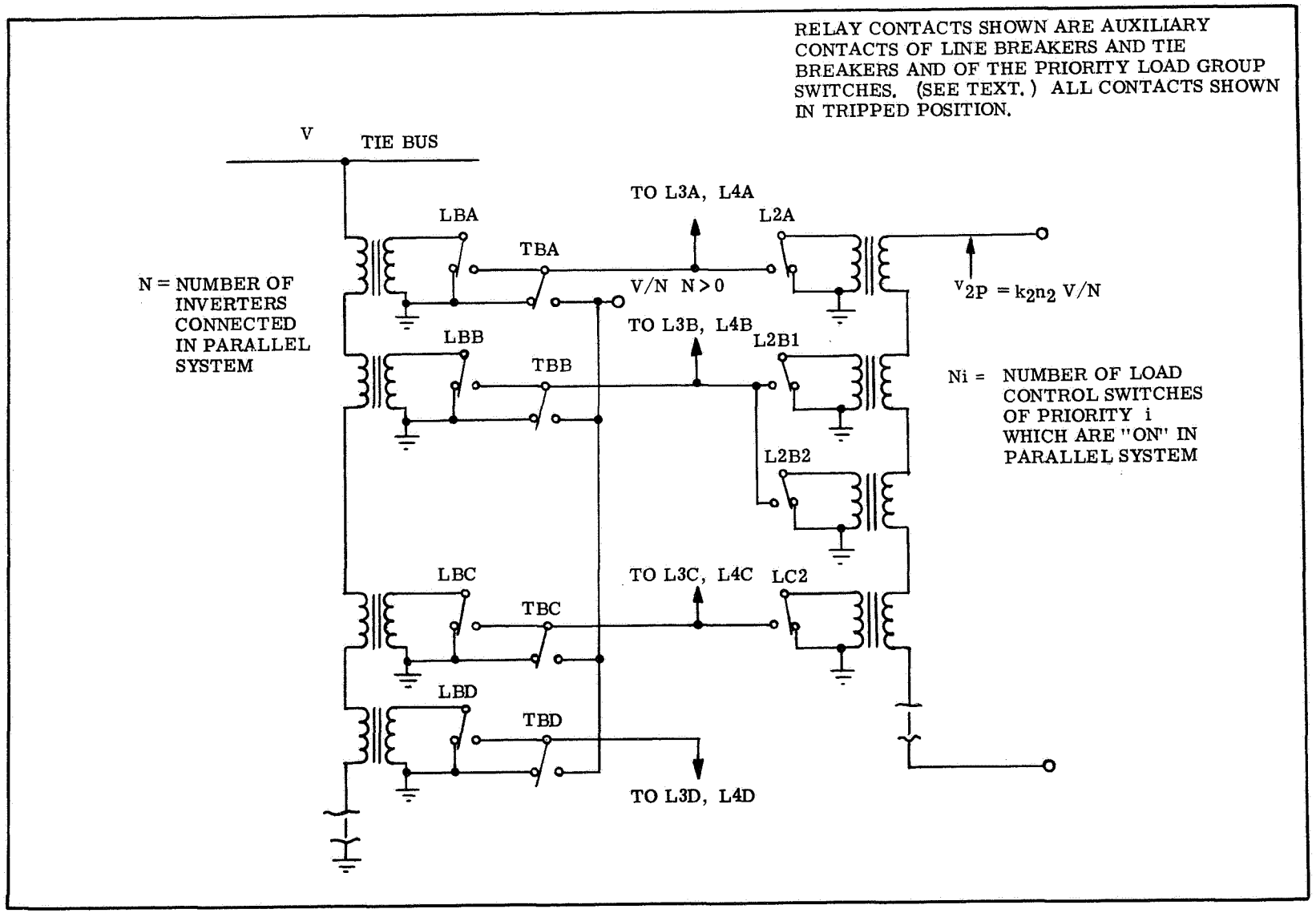


Figure 4. - Line Diagram of Load Anticipation Circuit (Parallel Operation)

which are the voltages required in the control circuits, equations (9), (17), and (20).

Load anticipation circuits for isolated inverters: When an inverter operates in an isolated mode, load programming is independent of the parallel system. The equations for the control voltages are of the same for, however, as those in the parallel system, but where $N = 1$.

For GO2A to exist

$$I_{1A} + I_{2A} + I_{2AP} < I_m$$

The control voltage equation is

$$v_{2A} + v_{2AP} < v_m$$

$$v_{2A} = kR(I_{1A} + I_{2A})$$

$$v_{2AP} = k_2 n_{2A} V_A$$

$$v_m = k_m I_m$$

$$kR(I_{1A} + I_{2A}) + k_2 n_{2A} V_A < k_m I_m$$

$$k_m = kR$$

$$k_2 n_{2A} V_A = I_{2AP}$$

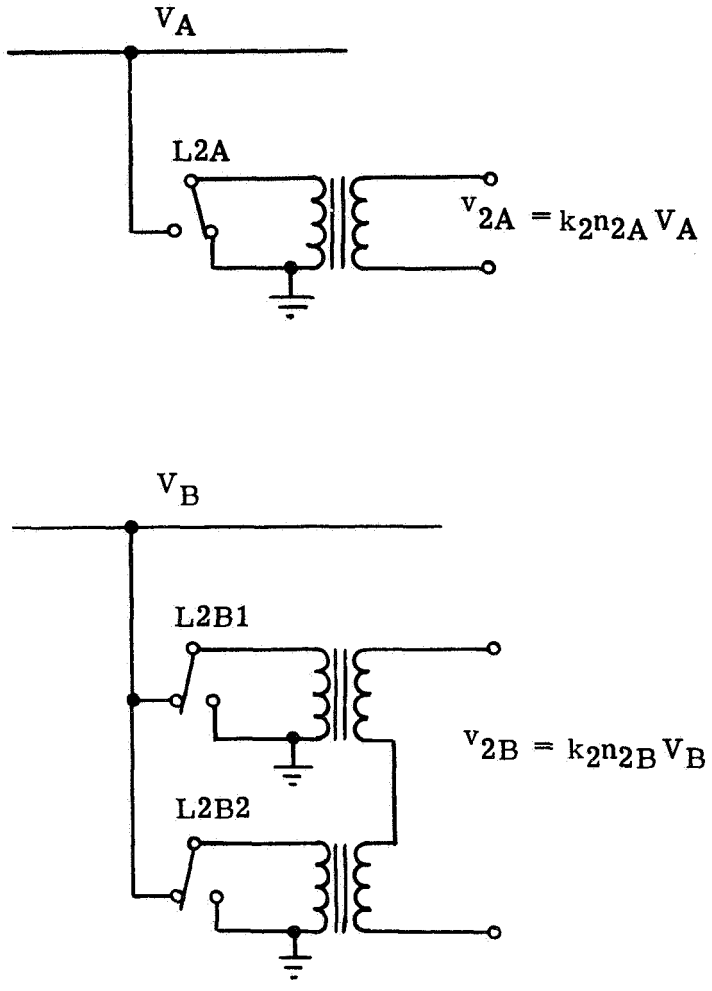
$$k_2 V_A = I_{2AP}/n_{2A} = I_{2P}/n_2 = k_2$$

Since normally $V_A = V$, assume the same transformer turns ratio as in the parallel system.

Figure 5 shows circuits for developing v_{2A} and v_{2B}. Each load group in the system requires a similar circuit for isolated load programming. The number of transformers in each circuit equals the number of load groups of a particular priority operating from a single load bus. Since v_{2A}, v_{3A}, etc., are not functions of N, these circuits are powered from the respective load busses. Output voltages from these circuits are

$$v_{2A} = k_2 n_{2A} V_A$$

$$v_{3A} = k_3 n_{3A} V_A$$



n_i = NUMBER OF LOAD CONTROL SWITCHES OF SAME PRIORITY AND SAME LOAD BUS IN "ON" POSITION.

EXAMPLE: IN CIRCUITS SHOWN n_{2A} MAY HAVE VALUES OF 0 OR 1; n_{2B} MAY HAVE VALUES OF 0, 1, OR 2.

Figure 5. - Line Diagram of Load Anticipation Circuit (Isolated Operation)

$$v_{4A} = k_4 n_{4A} V_A$$

$$v_{2B} = k_2 n_{2B} V_B$$

$$v_{3B} = k_3 n_{3B} V_B$$

$$v_{4B} = k_4 n_{4B} V_B$$

etc.

Summary of switching logic. - Logic equations for load switching were previously stated for the loads connected in the parallel system and in the isolated system. Noting that the position of the tie breaker determines whether parallel or isolated signals apply, the equations may be combined to apply to either condition. The general logic equations are as follows:

$$TRIP(i)(X) = \left[OL(i) \cdot TB(X) + OL(i)(X) \cdot \overline{TB(X)}\right] + \overline{(i)\ (X)}$$

TRIP OUTPUT SIGNAL = T(i)(X)

$$CLOSE(i)(X) = \left[GO(i) \cdot TB(X) + GO(i)(X) \cdot \overline{TB(X)}\right] \cdot (i)(X)$$

In the equation, (i) designates load priority, (X) identifies the load bus, and TB(X) is a logic signal indicating that the tie bus breaker is closed.

Alternative Approach Using Static Circuits

An alternative to the transformer-relay approach of generating control signals for the load programmer is to use static circuits to perform the necessary logic switching functions. Figure 6 shows the various elements of the load programmer sensing, logic, and comparator circuits for a four-channel parallel system.

The current-monitoring-circuits portion of figure 6 provides equivalent function to that of figure 3. Signals v_2, v_3, and v_4 provide analog information as to the magnitude of current to each of various combinations of priority load groups. These signals, in conjunction with others, are used to determine when loads are added to or removed from the parallel system.

The load-anticipation-monitoring-circuits portion of figure 6 provides an equivalent function to that of figure 4. Signals v_{2P}, v_{3P}, v_{4P} are analog signals indicating the magnitudes of loads of

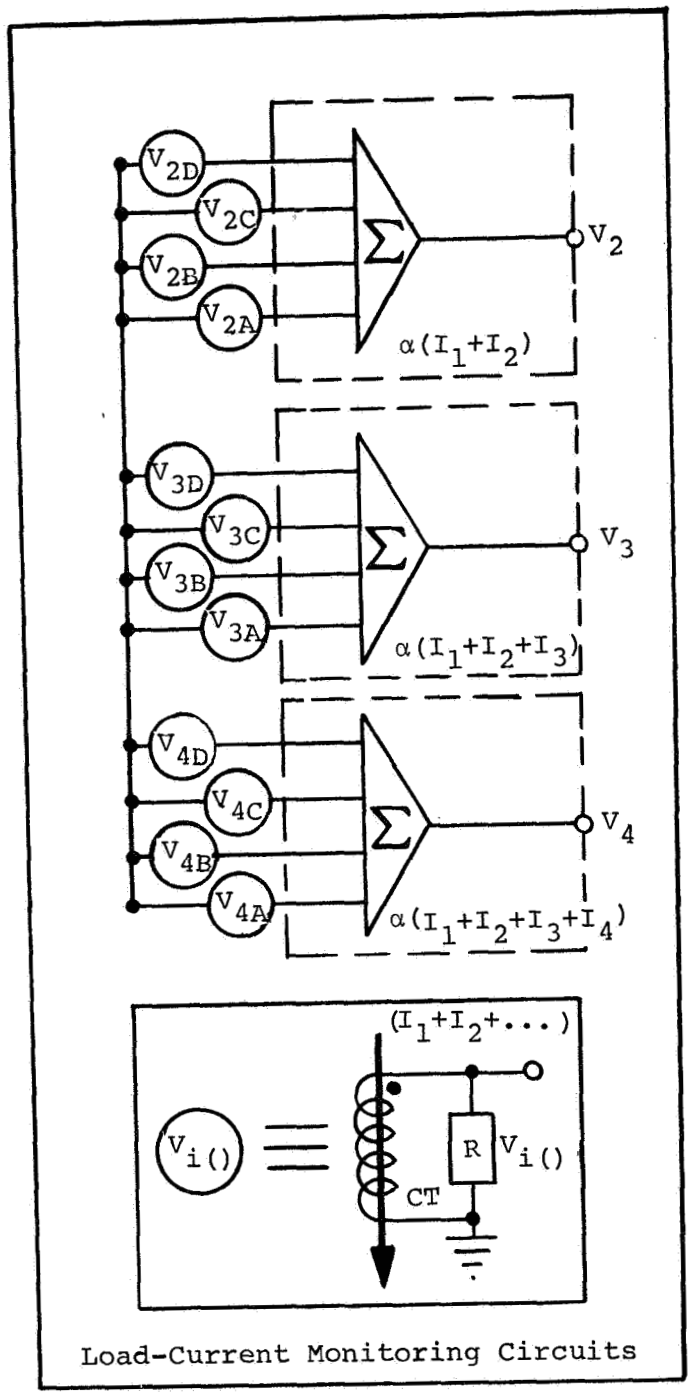


Figure 6. - Replacement of Relay Circuits with Static Circuits for Load Programmer

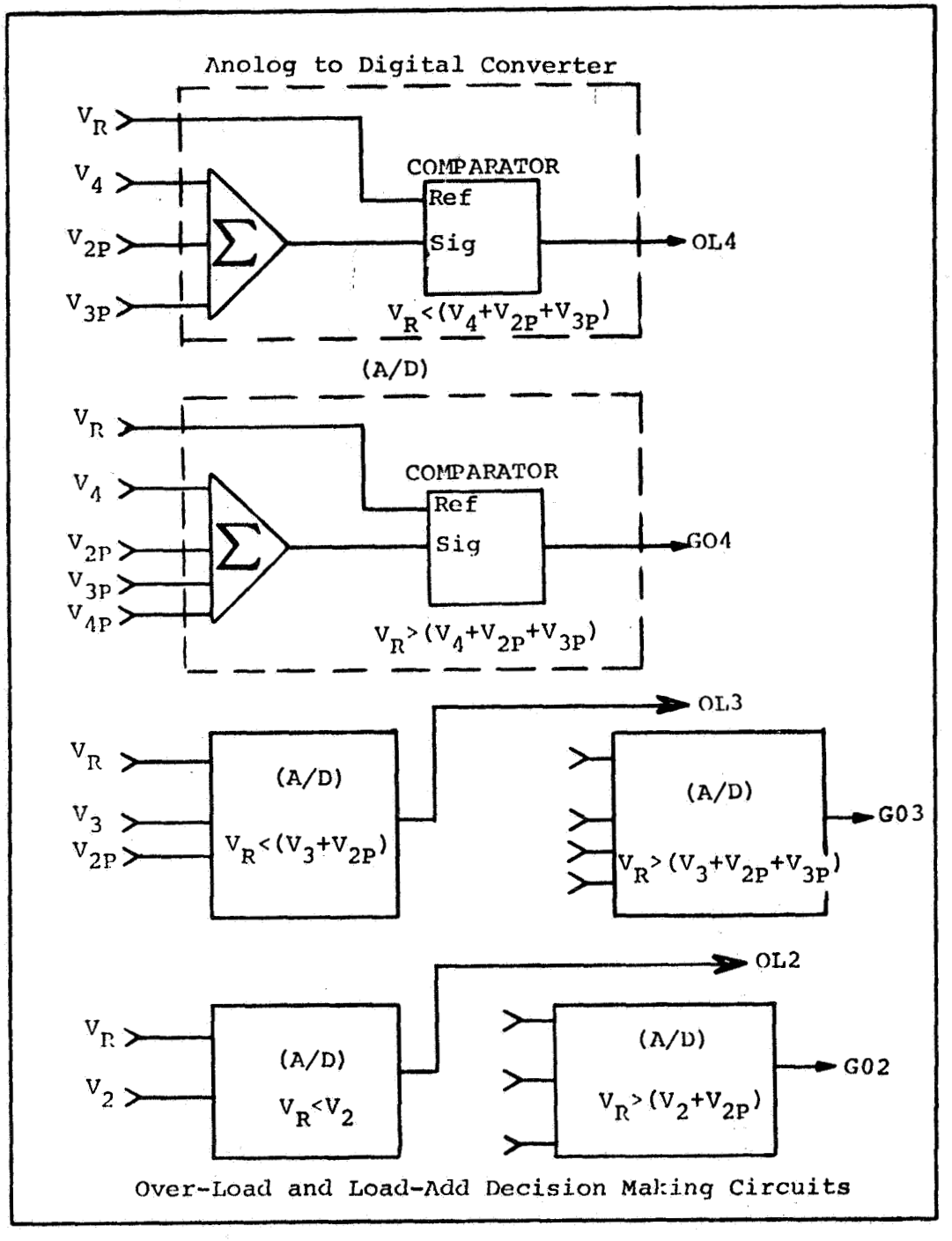


Figure 6. - Continued

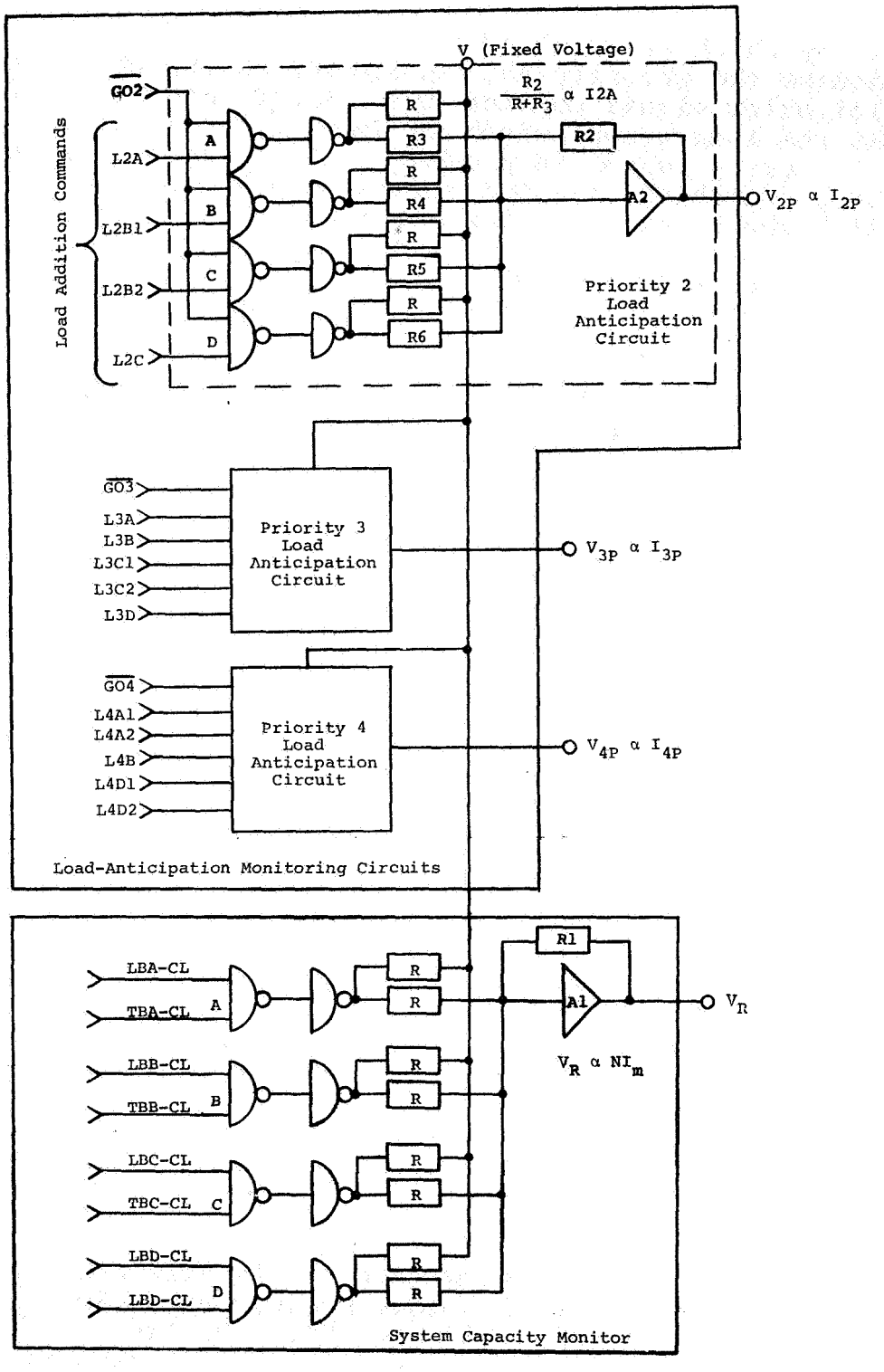


Figure 6. - Concluded

each priority which are desired to be connected to the system but cannot because the priority load group switch is not closed. The load anticipation signal depends upon 1) the magnitude of the load, 2) whether the load-group switch is open, and 3) whether a command to close the group switch is present. As the equations for closing a load-group switch show, a GOi signal must be present if a load-group switch can be closed. Hence, requirements 2 and 3 are met by a NOT GOi signal and a Li( ) command signal as shown in figure 6. The analog signal proportional to current to be added is derived by the value of the input resistors and feedback resistor of the summing amplifier A2.

These two circuits described above provide information as to the magnitudes of actual and desired loads on the system. All that remains is to derive an analog signal proportional to the operating capacity of the parallel system. The system capacity monitor of figure 6 provides this information. A voltage proportional to the rated current of each system is connected to a summing amplifier whenever both the tie breaker (TB) and load breaker (LB) are closed. The output of the summer (signal V_R) is then proportional to system capacity.

We now have all the elements necessary to generate close and trip signals for the load-group switches. The signals GOi and OLi are dependent on the comparison of actual and expected currents to the available capacity of the parallel system. The analog-to-digital (A/D) converters of figure 6 sum the appropriate signals and compare them to the system capacity signal V_R. The output of the A/D converters is used to trip or close the various load-group switches as defined in the summary equations.

Reliability Considerations

The effect of a load programmer on the reliability of an electric power system is essentially the same as adding the control and protection circuits described in the report entitled "Inverter-Converter Automatic Paralleling and Protection" (ref. 2). Because the load programmer was a conceptual study, no reliability calculation can be presented. However, the following general statement can be made.

Obviously, if no failures within an electric power system can be tolerated, the addition of a load programmer would only degrade system reliability. However, if variations in the amount of system capacity can be tolerated and there are several categories (or priorities) of loads on the system, the system can be made more reliable by the addition of a load programmer. This comes about because of added system flexibility in terms of loads connected to the power system and by the ability to compensate for variations in system power capacity.

Load Programmer Concluding Remarks

An electrical circuit concept has been developed for a load programmer to be used in a three-phase electric power system utilizing multiple static inverters. This programmer automatically determines whether the electrical loads exceed the capacity of the paralleled-inverter system. When the capacity is exceeded, low-priority loads are automatically removed until the system capacity is not exceeded. If the capacity is not exceeded, the programmer establishes conditions which permit loads to be applied.

Such a load programmer concept may be very useful in future space vehicles where a parallel system with multiple load busses is used and where electric power is maintained to high priority loads even though individual parts of the parallel system may malfunction or fail. With a load programmer and a parallel system, failures within the electric system will not result in complete, catastrophic failure of the space mission.

STATIC SWITCHES

Description

Systems as described in reference 2 required many electrical contactors. Figure 7 shows the layout of a system similar to the system analyzed in reference 2. This portion of the study was to develop concepts and breadboard hardware to replace the mechanical contactors with ac and dc static switches.

Generally, faults can appear in any location of an electrical power system from the energy source to the end point of load utilization. Consequently, the contactors must be rated accordingly. In single or isolated subsystem operation, the ICC/CCC, LBC, and LCC are rated for a one per unit steady state load capacity, plus normal overloads, with a fault capability as determined by the inverter/converter current limiting characteristic. In the general case of the paralleled inverter/converter system, the LBC, LCC, and TBC must be rated to permit the conduction of current from the overall paralleled system for faults which occur within the subsystem. The fault power ratings of these contactors, therefore, are a function of the number of paralleled subsystems, with the LBC and TBC rated identically to account for a fault which may result, such as at point A in figure 7.

The fault power rating of the LCC, in paralleled system operation, is greater than the LBC and TBC because of faults which could occur at point B in figure 7, resulting in current from its associated power source and the overall system through the TBC. The rating of the ICC/CCC is the same for parallel operation as it is for single subsystem operation.

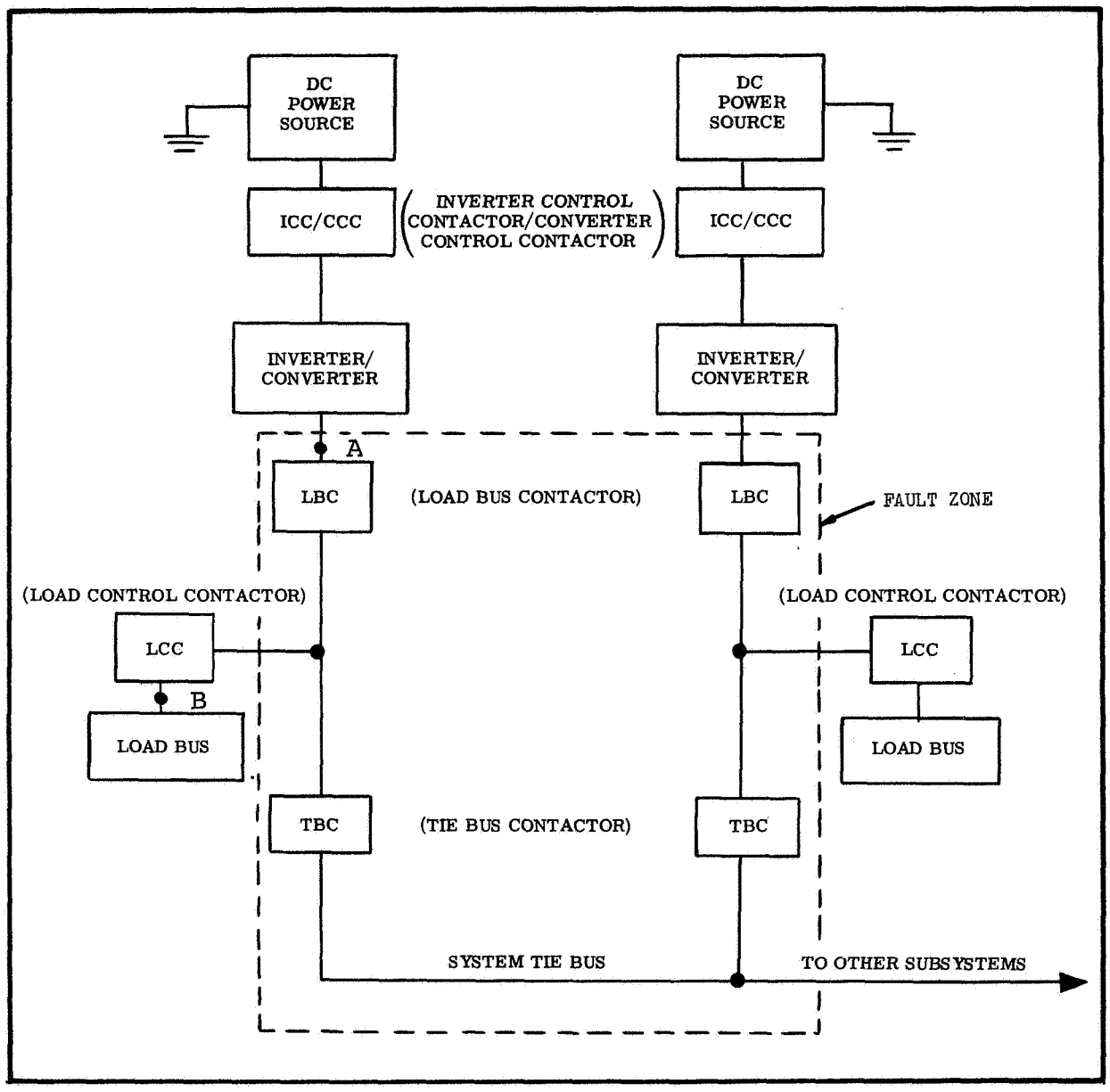


Figure 7. - Paralleled Inverter/Converter System Block Diagram

The static contactors for this program have been designed for faults which are limited to a zone from the output side of the inverter/converter to the system tie bus and up to the inverter/converter side of the LCC. This fault zone is shown enclosed by dotted lines in figure 7.

In the given two inverter/converter subsystem the power ratings of all the contactors considered are the same for parallel system operation as for single subsystem operation. Therefore, the static contactor power ratings for the LBC, LCC and the TBC, for this two parallel inverter/converter program, are equal and, with the exception of the converter system TBC, are identical to each other in their respective systems. The difference between the converter system TBC and the identical designs of the converter LBC and LCC is that the TBC must provide for bilateral power transfer while the LBC and LCC are designed for unilateral power transfer. Although all three of the contactors, on the converter output, will use the same electrical components, the TBC will use an additional silicon controlled rectifier contact, with its control circuit, to permit the flow of power form the paralleled output bus to its associated subsystem load. In the general case, the converter LBC should also provide bilateral power transfer, similar to its electromechanical counterpart, for fault clearing such as point A in figure 7.

Fundamentally the static contactor is made up of two parts, a power circuit and a control circuit. The power circuit, consisting of a switching device, permits the conduction of current from the source to the load when activated. The control circuit provides the necessary turn-on and turn-off requirements from input signals. Input signals are provided whenever one of the following conditions exists:

1) current is demanded at the load,

2) current is no longer required by the load, and

3) when abnormal electrical system operation prevails in a protected zone.

Voltage and Current Specifications

The inverter/converter normal system voltages and currents and the system abnormal currents which the static contactors must withstand and open are shown in tables I and II. The electrical specifications given in tables I and II are specifically for a two channel parallel system. The design philosophy regarding the silicon controlled rectifier contact current is to provide a steady state capability of two times rated inverter/converter system current and

Table I. - Converter System Static Contactor Current and Voltage Specification

Converter Rating (nominal) Capacity 750 watts Voltage 153 volts Contactor Voltage and Current Rating	CCC	LBC	TBC	LCC
Rated Voltage (volts, avg.)	28±2	153±5	153±5	153±5
Rated Current (amps, avg.)	40	4.9	4.9	4.9
Normal Overload Current, 125% 5 Minutes (amps, avg.)	50	6.13	6.13	6.13
Maximum Short-Circuit Current Steady State, 150% (amps, avg.)	60	7.35	7.35	7.35
Maximum Duration Short-Circuit Current (milliseconds)	600	600	175	----
Maximum Peak Transient Current (amps)	215	16.5	16.5	16.5
Design, Rated Current, 200% (amps, avg.)	80	9.8	9.8	9.8
Design, Short-Circuit Current Steady State, 250% (amps, avg.)	100	12.3	12.3	12.3
Design, Short-Circuit Time (milliseconds)	1000	1000	1000	1000

250 percent short-circuit current. The contactor design selection for a short-circuit capability of 250 percent, with fault times in excess of those necessary for integrated system protection, is compatible with the inverter/converter steady-state current design limitation of 150 percent.

The controlled rectifier contact voltage will be rated for a minimum of two times the highest voltage it is likely to see during operation.

Table II. - Inverter System Static Contactor Current and Voltage Specification

Inverter Rating (nominal) Capacity 750 volt-amperes Voltage 115/200 volts, 400 Hz Contactor Voltage and Current Rating	ICC[(a)]	LBC	TBC	LCC
Rated Voltage (volts, L-N, rms, 400 Hz)	28±2	115±6	115±6	115±6
Rated Current (amps, line, rms, 400 Hz)	40	2.18	2.18	2.18
Normal Overload Current, 125% 5 Minutes (amps, rms)	50	2.73	2.73	2.73
Maximum Short-Circuit Current Steady State, 150% (amps, rms)	60	3.27	3.27	3.27
Maximum Duration Short-Circuit Current (milliseconds)	215	215	175	----
Maximum Peak Transient Current (amps)	215	8	8	8
Design, Rated Current, 200% (amps, rms)	80	4.36	4.36	4.36
Design, Short-Circuit Current, Steady State, 250% (amps, rms)	100	5.45	5.45	5.45
Design, Short-Circuit Time (milliseconds)	1000	500	500	500

(a) The ICC requirements are identical to those for the CCC given in table I. The currents and voltages for the ICC, therefore, are dc average values with exception of the transient current which is a peak value.

Characteristics of Power Switching Device

The qualities exhibited by the silicon controlled rectifier include extremely high forward and reverse blocking voltages which are in excess of 1300 volts with typical peak leakage currents of two microamperes to ten milliamperes at a junction temperature of 25°C. The higher voltage rated controlled rectifier devices have lower leakage currents for a given forward current rating.

Voltage transients in the forward direction and to some extent in the reverse direction that exceed the rated blocking voltage are protected by the inherent characteristics of the device. Overvoltage in the forward direction will cause the device to break down into the conducting state, and, if the rate of change of current and peak current is limited, the device suffers no ill effects. These quantities can be controlled in practical circuits. The circuit, however, must withstand this breakdown conduction.

The main destruction mechanism of a controlled rectifier is excessive current density in the forward direction. This is tempered with the relatively high, short-time overcurrent ratings of the device, typically 5 to 8 times the peak rated repetitive current rating of the device.

The silicon controlled rectifier is capable of being turned on with a 1 to 10 microsecond pulse. Turn-off time is 5 to 25-30 microseconds. The device has a 1 to 1.5 volt forward drop and a maximum junction temperature rating of 125°C.

The major disadvantage of the controlled rectifier is its recovery mechanism. The device is controlled by its gate lead when it is required to switch from a blocking to a conducting state, but the gate lead no longer has control when the controlled rectifier is conducting.

The direct current contactors of this application must use forced commutation means to regain the blocking state while the alternating current contactors can rely on natural commutation since the current goes to zero every half cycle. The forced commutation process requires high surges of energy in the power circuits, as provided by reactive energy storage elements. Thus, the controlled rectifier turn-off components tend to be large and bulky.

Converter System Contactor Circuit Considerations

The design of the converter system static contactors requires consideration of a direct current system only. The following is a discussion of the power circuit configurations.

DC static contactor with capacitor turn-off. - A fundamental contactor circuit which uses capacitor, forced-commutation, turn-off of the controlled rectifier contact is shown in figure 8. Supply voltage V is applied to the load by application of a turn-on signal from gate to cathode of silicon controlled rectifier SCR1. With SCR1 conducting, capacitor C is charged to the supply voltage, less the voltage drop across SCR1, through resistor R. The left plate of the capacitor is charged with a positive polarity. To turn SCR1 off, removing the voltage from across the load, SCR2 is turned on. This connects the negative side of capacitor C to the anode of SCR1. This reverse biases SCR1 momentarily resulting in turn off. Capacitor C now becomes charged to essentially the supply voltage (less the voltage drop across SCR2) with a positive polarity on its right plate. Controlled rectifier SCR2 continues to conduct at minimum current through R. When SCR 1 is turned on again, with a signal from gate to cathode, the circuit reverts to its original state with SCR2 turned off after being reverse biased by capacitor C.

The disadvantage of this circuit is that, momentarily, two times supply voltage is applied across the load when SCR1 is commutated.

DC static contactor with resonant circuit turn-off. - A contactor power circuit which eliminates the load voltage rise objection of figure 8 is shown in figure 9. With exception of the addition of inductor L and diodes CR1 and CR2, the circuit configurations of figures 8 and 9 are identical.

In figure 9, with SCR1 conducting, voltage is applied to the load and capacitor C1 is charged to the supply voltage V less the voltage drop across SCR1. The left plate of the capacitor, therefore, is at a positive polarity. To turn SCR1 off, SCR2 is turned on. This provides a path for C1 to discharge resonantly through SCR1 or CR1, SCR2 and L. The discharge current is one alternation of a sine wave. Until the capacitor discharge sine wave current reaches the magnitude of the load current, the effect of the discharge is to reduce the current through SCR1. When the capacitor current reaches and exceeds the original value of SCR1 load current, the excess current flows through CR1, reverse biasing SCR1 and turning it off. Capacitor C1 now completes its charge to the supply voltage, less the SCR2 voltage drop, with a positive polarity on the right plate. The capacitor cannot discharge again because CR1 and SCR1 are blocking. Controlled rectifier SCR2 continues to conduct through resistor R. To revert to the original state, with SCR1 conducting, SCR1 is turned on and capacitor C1 discharges through L, SCR2 or CR2, and SCR1. This turns SCR2 off, and SCR1 conducts current to the load.

The objection to this circuit, as presented, is its inability to open when closed onto a short circuit. When a system short-

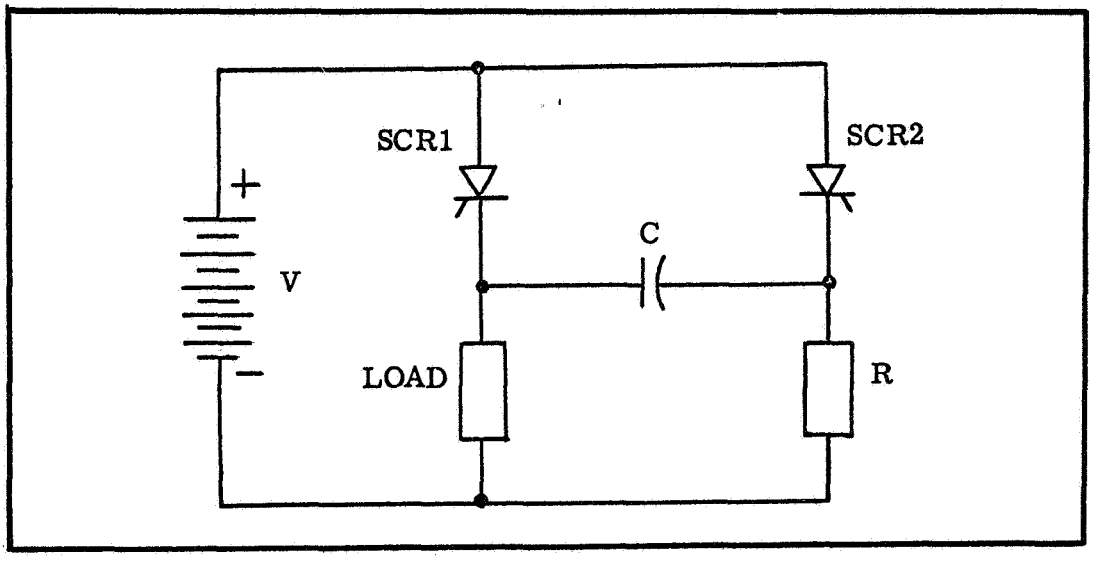


Figure 8. - DC Static Contactor with Capacitor Turn-Off

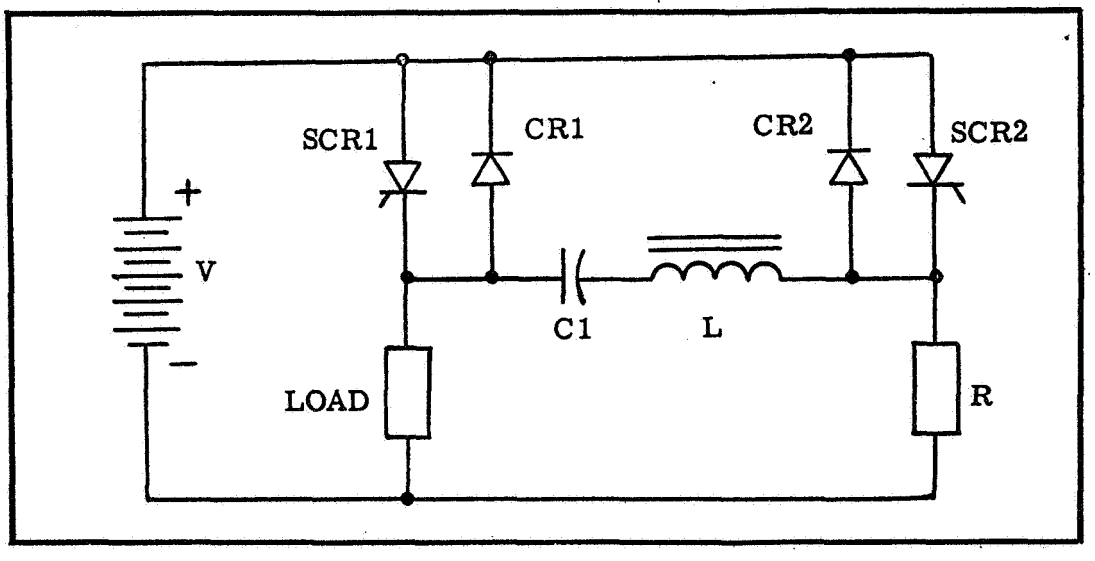


Figure 9. - DC Static Contactor with Resonant Circuit Turn-Off

circuit fault occurs, the converter output voltage droops and essentially attains a zero value because of the current limiting characteristic of the inverter/converter. Should this fault persist after the contactor has been opened the first time, the contactor will not open again if it is closed. The reason for this is that with the immediate depression of the converter output voltage to essentially zero, capacitor C1 cannot become charged. Although SCR2 can be turned on, by the appropriate signal, SCR1 cannot be turned off and therefore will continue to conduct until it or some other system equipment is destroyed by fault current.

DC static contactor with resonant circuit turn-off capacitor with independent charging provisions. - Contactor circuits of figures 10 and 11 provide a means of initially charging commutating capacitor C1 prior to the time SCR1 is turned on. Figure 10 is the same as figure 9 with the exception that SCR3 has been added to the power circuit in series with SCR1 and the load. When SCR1 is turned on, it will charge capacitor C1 through L and R. After a time delay, which is a function of R2 and C2, SCR3 turns on applying voltage to the load. Controlled rectifier SCR1 turn-off occurs as discussed for the circuit of figure 9. Controlled rectifier SCR3 turns off naturally when the current through it decreases below the holding current because of SCR1 turning off.

The disadvantage of this circuit is the increase in steady-state power losses to twice those of figure 9.

The circuit of figure 11 overcomes the disadvantages of the circuit of figure 10 by rearranging the charging path of turn-off capacitor C1. The basic operation of this circuit is the same as described for figure 9 except that capacitor C1 is charged through CR3, L, and R from the dc control bus when SCR1 is turned on. Capacitor C1 completes its charge, with its left plate positive, before SCR1 is turned on because of a time delay in the SCR1 gate-to cathode control circuit. If the contactor has not closed on a short-circuit, the voltage across the load will be normal and the initial charge on capacitor C1 will be maintained by conduction of diode CR2. Without diode CR2 capacitor C1 could lose its intitial charge through self leakage.

Because the circuit of figure 11 provides the advantage of turning off the contactor under a short-circuit condition without a decrease in steady-state efficiency, it was selected for the ICC/CCC.

To turn SCR1 off, because of a fault or normal system shutdown, turn-on signals are provided simultaneously to SCR2 and SCR3. The turn-off operation is then the same as discussed for figure 9. Controlled rectifier SCR2 continues to conduct minimum current through R. Controlled rectifier SCR3 turns off naturally after C1

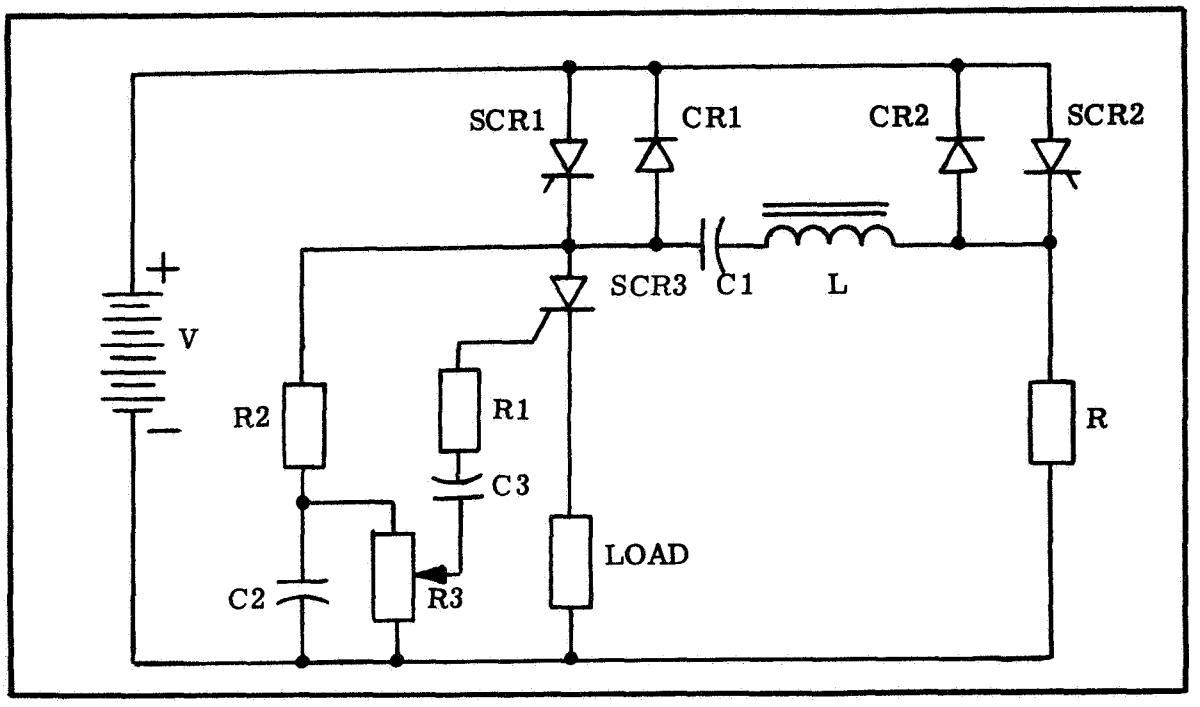


Figure 10. - DC Static Contactor with Resonant Circuit Turn-Off with Independent Capacitor Charging Provisions

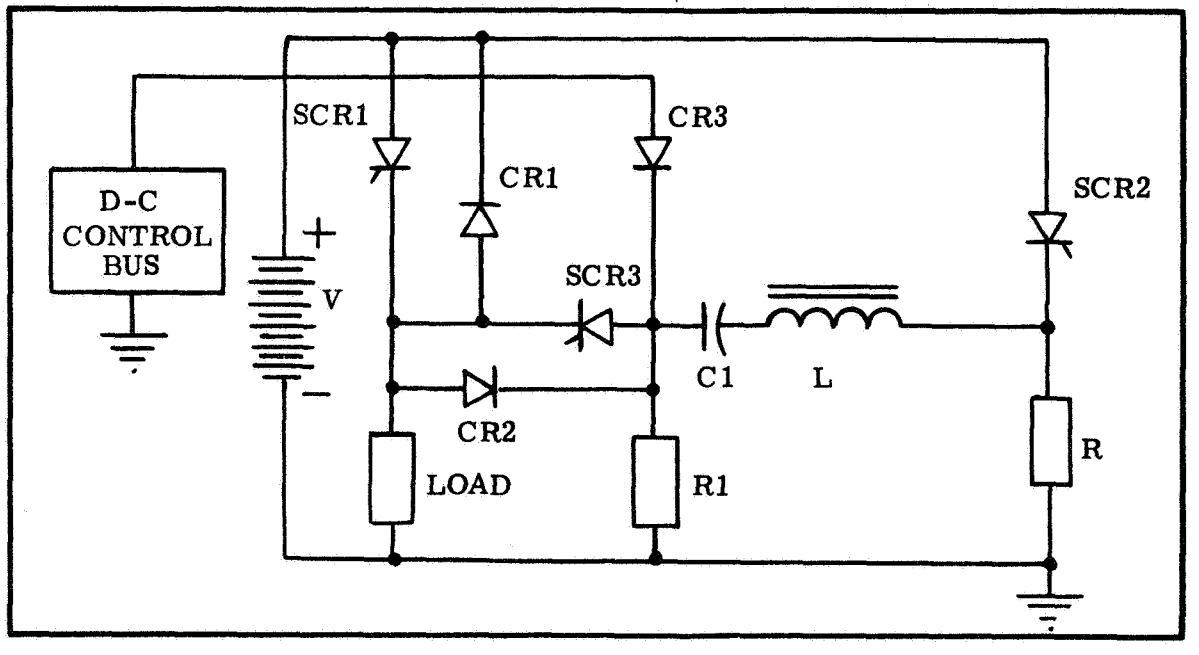


Figure 11. - Selected DC Static Contactor Circuit

charging current decreases to a value below the minimum holding current of SCR3. The capacitor is now charged with its right plate at a positive polarity. This charge is maintained through the high resistance path provided by R1. To return to the original condition, with SCR1 conducting, SCR1 is turned on. Prior to SCR1 turning on, the dc control bus voltage is connected in series with CR3, C1, L, and R. The potential at the cathode of SCR2 will attain a value which will exceed that at the anode. This reverse biases SCR2, resulting in turn-off.

Converter System Contactor Designs

Inverter control contactor/converter control contactor. - The complete circuit diagram for the ICC/CCC is shown in figure 12.

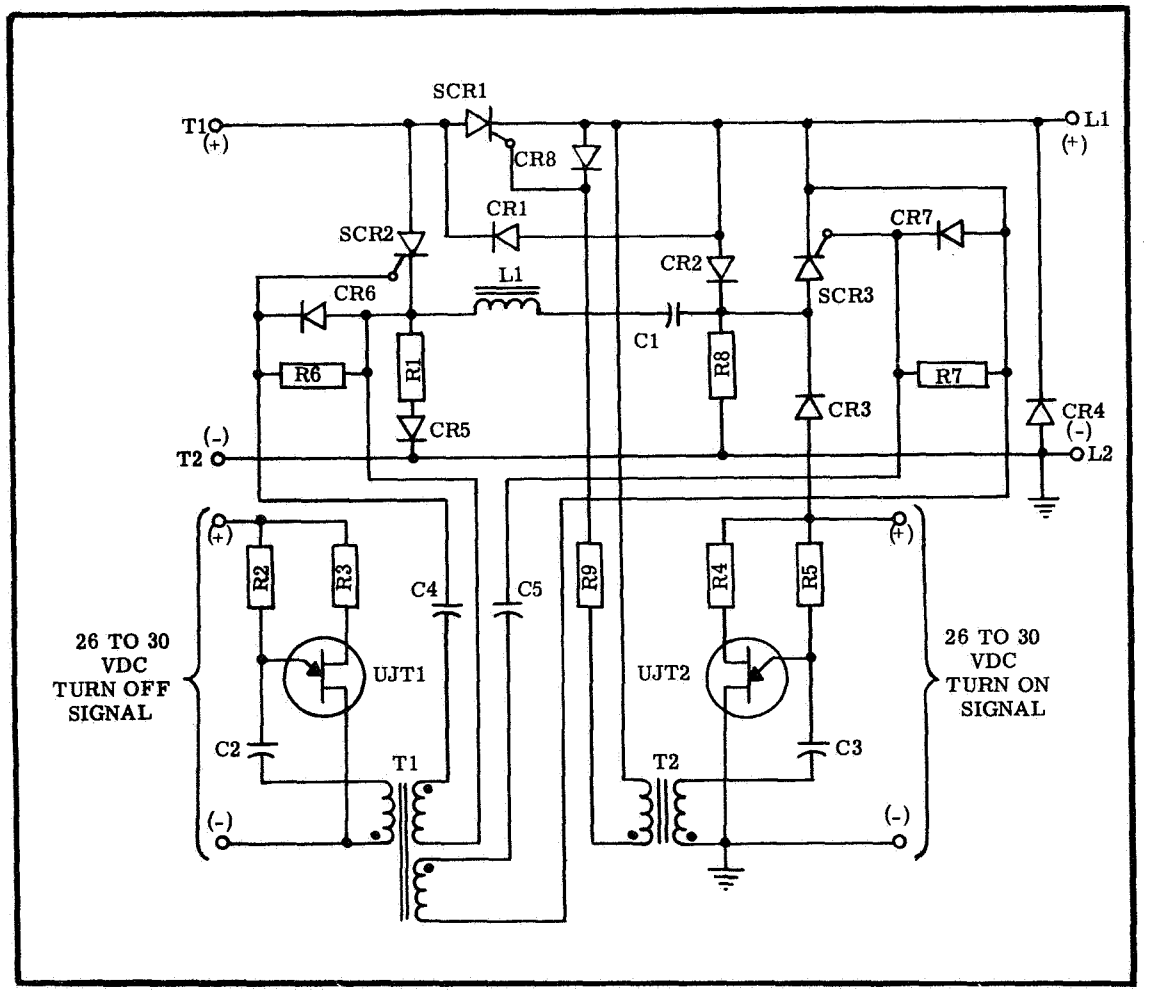


Figure 12. - Static Inverter Control/Converter Control Contactor Circuit

Free-wheeling diode CR4 has been added across the load side terminals L1 and L2 of the contactor to provide a path for circulating inductive currents when the contactor is opened. Diode CR5 is in series with R1 to prevent the initial energy of C1 (resulting from the turn-on signal) from discharging prior to SCR1 turning on.

Since the operation of the power circuit was described previously, the following discussion will be limited to the description of the control circuits. In addition, because the control circuits for turn-on and turn-off are basically the same, only the turn-on circuit will be discussed. The principal difference between the two control circuits is in the pulse transformers which show a single secondary for the turn-on configuration and two isolated secondary windings for the turn-off configuration.

The control circuits consist of unijunction transistors operating in a relaxation oscillator mode. With the input to the turn-on circuit momentarily connected to the direct voltage control bus, capacitor C3 starts to charge through resistor R5. After a time delay, which has permitted C1 to become charged through diode CR3, the voltage across C3 reaches a potential which causes the unijunction transistor UJT2 to conduct through the emitter to base 1 circuit. This provides a pulse to transformer T2 which causes SCR1 to conduct. The controlled rectifier gate pulse continues until the discharge of capacitor C3 reaches a reduced voltage which causes UJT2 to cut off. Capacitor C3 is then charged again to a potential which causes UJT2 to conduct. The cycle is repeated and will continue as long as an input signal is provided. When the control circuits are intially energized, the current through the pulse transformers is in a direction which places a reverse voltage on the gate-to-cathode of the controlled rectifiers. The addition of diodes CR6, 7, and 8 in the gate-to-cathode circuit of controlled rectifiers SCR1, 2, and 3 clamps the negative or reverse gate-to-cathode signal to the forward drop of the diodes. A photograph of the breadboard design of the ICC/CCC is shown in figure 13.

Load bus, load control and tie bus contactors. - The circuit configuration for the converter system LBC and LCC is presented in figure 14, while figure 15 shows the schematic diagram for the TBC. The power circuit for these three contactors, on the converter output side, uses the capacitor turn-off technique for SCR commutation. It is necessary to apply this circuit design to the converter output contactors when consideration is given to integrating the LBC and TBC into the converter system. With the ICC/CCC circuit applied to the LBC, the diode in parallel with the power contactor SCR would prevent the isolation of a fault from the parallel system bus should a fault occur between a subsystem converter and the LBC, such as at point A of figure 7. Using the basic power circuit of the ICC/CCC, in a bilateral conducting configuration, the convential diodes would be connected in parallel

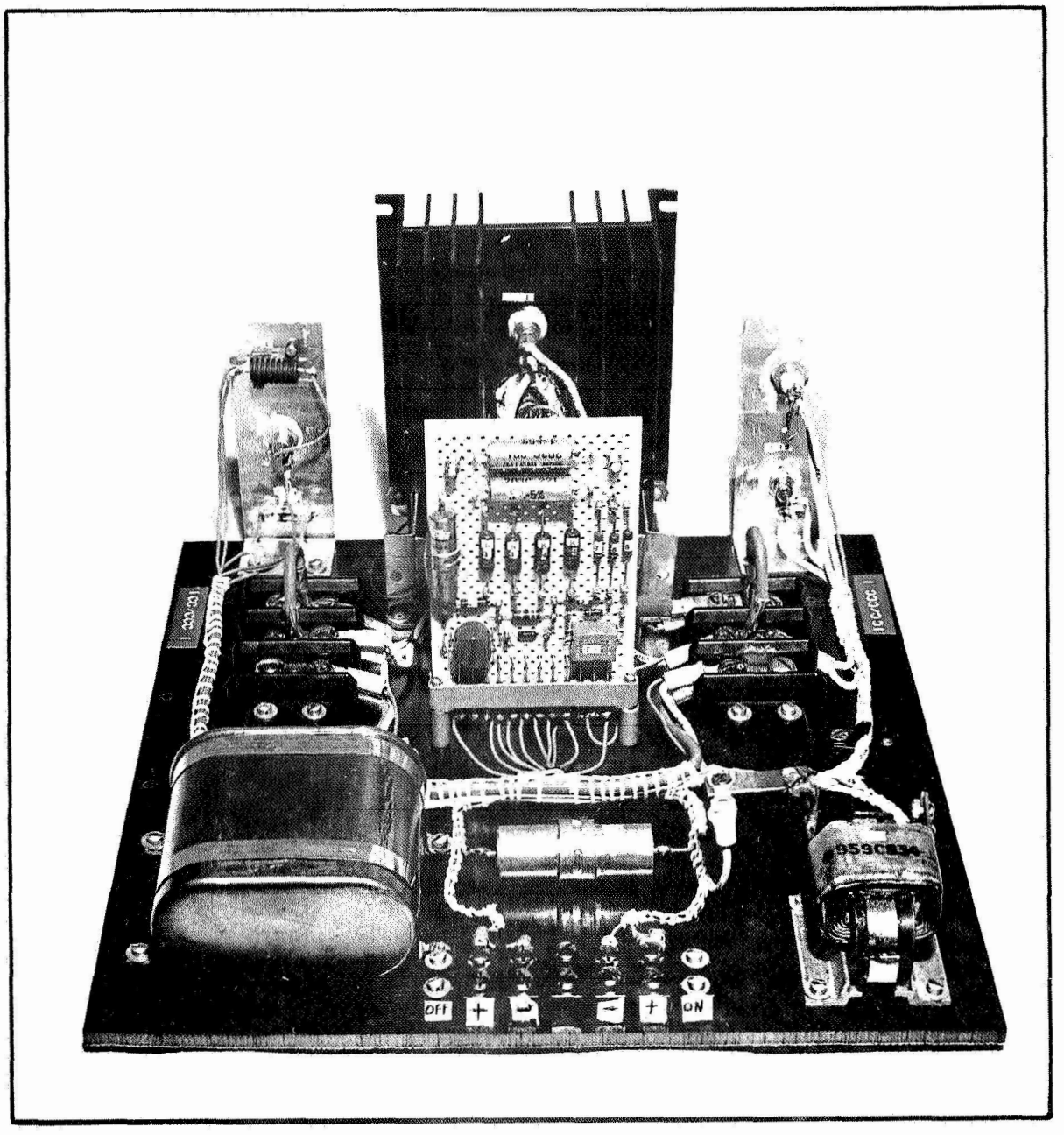


Figure 13. - Engineering Verification Model of ICC/CCC

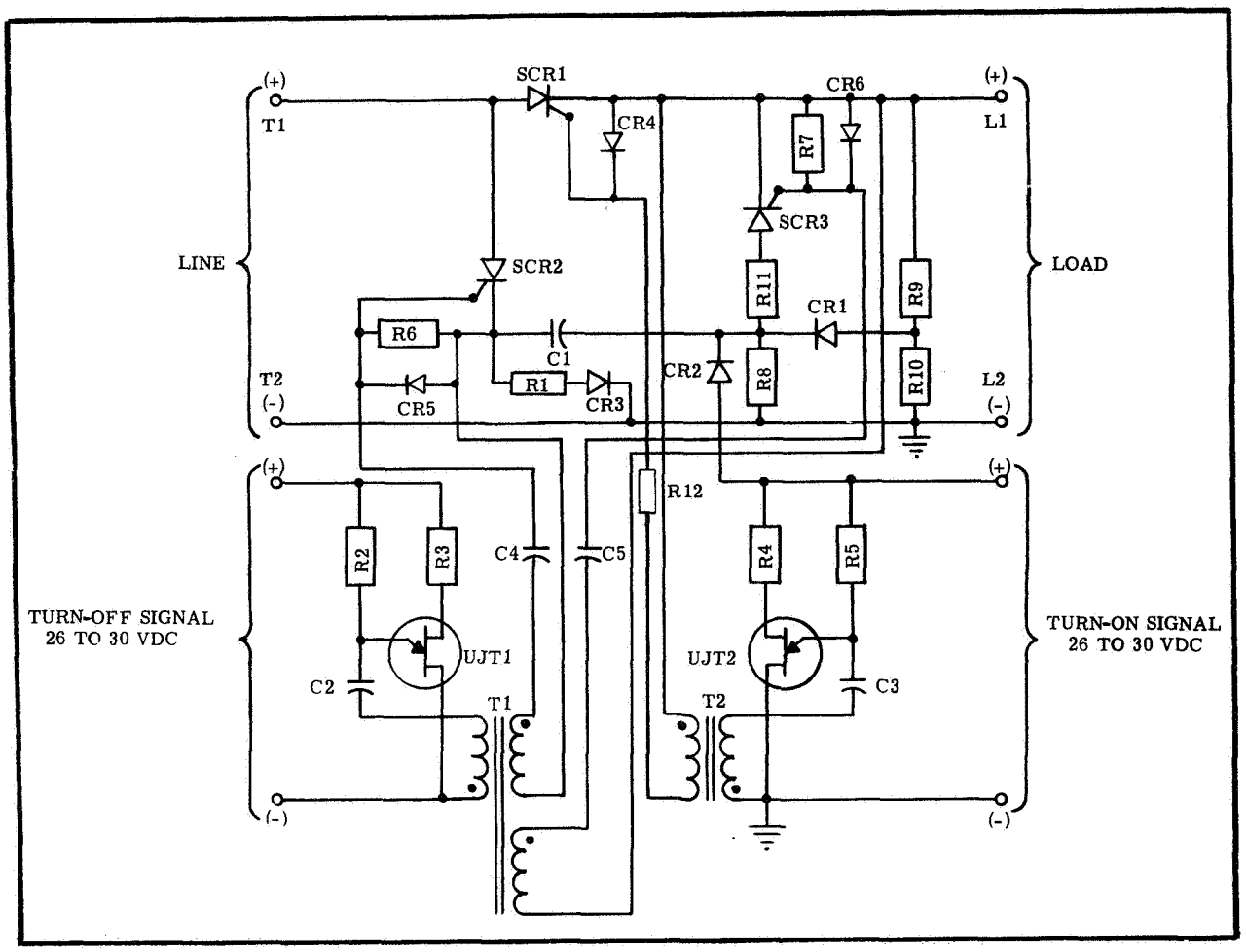


Figure 14. - Converter System Static Load Bus and Load Control Contactor Circuit

opposition with the SCR power contacts such that the TBC would always be closed through these parallel diodes.

The disadvantage of load voltage rise with the capacitor turn-off contactor design has been significantly reduced, on a percentage basis, by charging the commutating capacitors to a maximum of only 30 volts. This is accomplished through use of resistor voltage dividers which are connected across the dc transmission line. Therefore, with a maximum of 163 volts on the dc output bus, during an overvoltage condition, a maximum voltage of 193 volts should occur across the load when either the LBC, LCC, or TBC are opened. This voltage transient is within the dc power system requirements of MIL-STD-704, Characteristics and Utilization of Aircraft Electric Power.

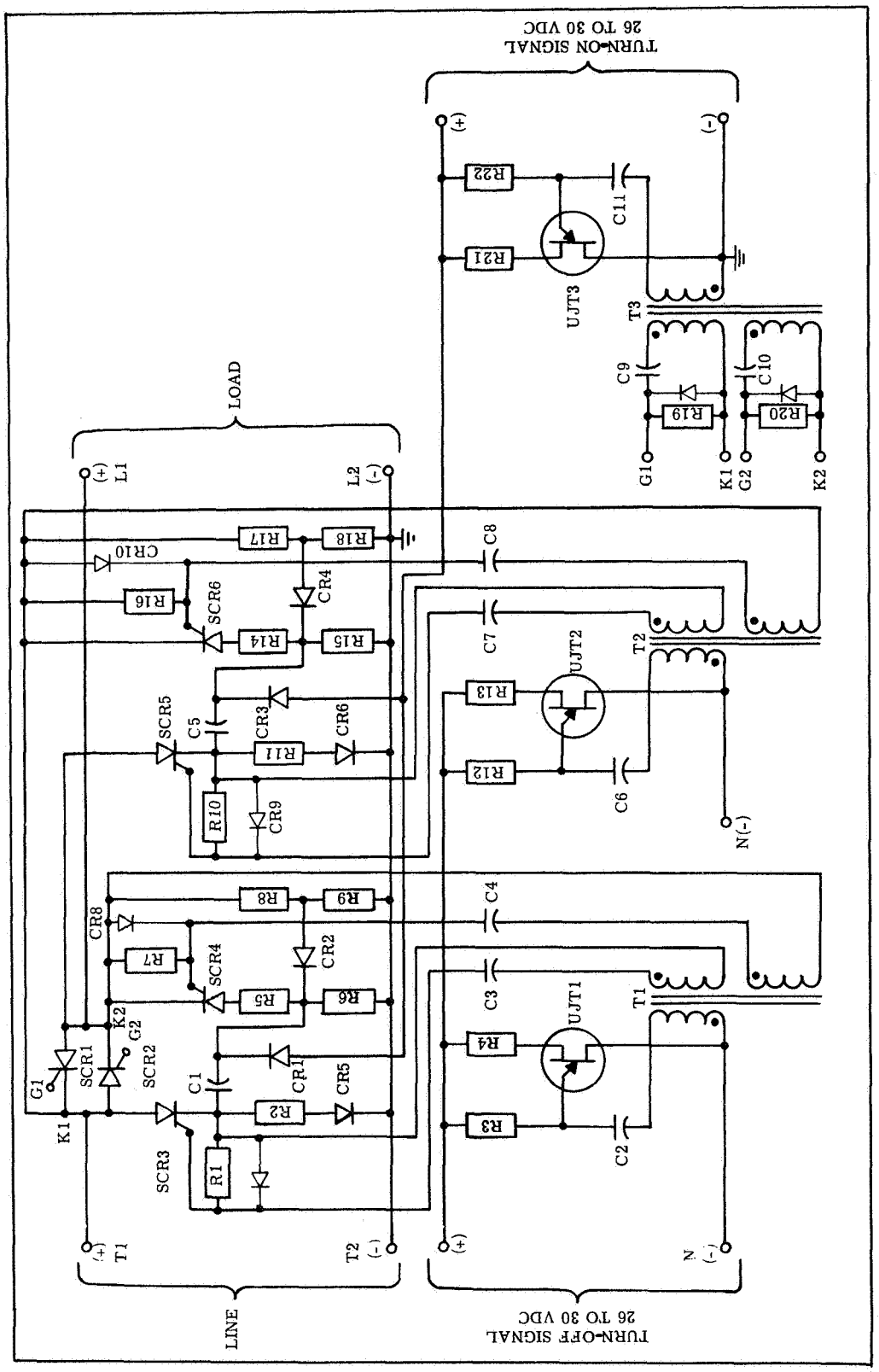


Figure 15. - Converter System Static Tie Bus Contactor Circuit

The circuit discussion which follows describes the power circuit only of the LBC and LCC of figure 14 since the control circuit is the same as for the ICC/CCC which was discussed previously.

With controlled rectifiers SCR2 and SCR3 off, capacitor C1 is charged through CR2, CR3, and R1, from the dc control bus when a momentary (less than one second) turn-on signal is provided for SCR1. Capacitor C1 completes its charge, with its right plate positive, before SCR1 is turned on because of the time delay in the SCR1 gate-to-cathode control circuit provided by R5 and C3. If the contactor has not closed on a short-circuit, the voltage across the load will be normal (line voltage of T1-T2 less the voltage drop across SCR1) and the initial charge on capacitor C1 will be maintained by conduction of diode CR1 through R9. Without the voltage divider R9 and R10 and CR1, C1 would lose its initial charge through self leakage. With SCR1 conducting, capacitor C1 is charged to the contactor input voltage less the voltage drop across SCR1 and the voltage drop across resistor R9.

To turn SCR1 off, because of a fault or normal system shutdown, turn-on signals are provided simultaneously to SCR2 and SCR3. This connects the negative side of capacitor C1 to the anode of SCR1. This reverse biases SCR1 momentarily resulting in turn off. Resistor R11 is used to limit the magnitude of the current in the capacitor discharge circuit. With SCR1 not conducting, capacitor C1 becomes charged essentially to the contactor input voltage T1-T2 with a positive polarity on its left plate. Controlled rectifier SCR2 continues to conduct minimum current through R1 and CR3 if this current is greater than the minimum holding current for SCR2. Controlled rectifier SCR3 turns off naturally after C1 charging current ceases. To return the contactor to the original condition with SCR1 conducting, SCR1 is turned on. Prior to SCR1 turning on, the dc control bus voltage is connected in series with C1 and R1 through CR2 and CR3. The instantaneous potential at the cathode of SCR2, if it is conducting, then becomes the sum of the control bus voltage and the voltage across C1. This reverse biases SCR2, resulting in turn off.

As seen in figure 15, the selected TBC design uses two controlled rectifiers connected in parallel back-to-back. The circuit discussion which follows describes only the power circuit of the TBC of figure 15 since the control circuit is similar to that of the ICC/CCC which was discussed previously. With controlled rectifiers SCR3, 4, 5, and 6 turned off, capacitors C1 and C5 are charged through their respective components CR1, CR5, and R2 and CR3, CR6 and R11 from the dc control bus when a turn-on signal is provided. For this contactor design, the turn-on signal is maintained as long as conduction is required for either direction. When the contactor is to be opened, system control and protection logic must first remove the turn-on signal and then apply the turn-off signal. With the turn-on signal applied, capacitors C1 and

C5 become fully charged, with their right terminals positive, before gating signals are provided to SCR1 and SCR2. This results because of the resistor-capacitor time delay of R22 and C11 in the turn-on circuit. If the contactor has not closed on a short-circuit, the system voltage will be normal and the initial charge on capacitors C1 and C5 will be maintained by conduction of CR2, CR5, and R8 and CR4, CR6, and R17 respectively. Without the voltage dividers R8-R9 and R17-R18 and the diodes CR2 and CR4, the commutating capacitors would lose their initial charge through self-leakage. With the system voltage such that SCR2 is conducting and SCR1 is not, capacitor C1 is charged to the contactor terminal voltage T1-T2 less the voltage drop across SCR2 and R8. The voltage across capacitor C5 will be charged to the contactor terminal voltage T1-T2 less the voltage drop across R17. The resulting capacitor voltage for C1 and C5 will be a maximum of 30 volts.

To open the contactor, a turn-off signal is provided after the turn-on signal has been removed. To eliminate the possibility of capacitor voltages C1 and C5 occurring simultaneously across the power contact SCR1-SCR2, a time delay has been incorporated into the unijunction circuit of UJT2 with components R12 and C6. This delay is sufficient to permit SCR2 to be turned off prior to gating SCR5 and SCR6 in the turn-off circuit of SCR1.

With the turn-off circuit energized, SCR3 and SCR4 turn on simultaneously. This connects the negative side of C1 to the anode and the positive side to the cathode of SCR2. This reverse biases SCR2 momentarily, resulting in turn off of the power contact SCR1-SCR2. With the power contact SCR1-SCR2 not conducting, capacitor C1 becomes charged to the contactor terminal voltage T1-T2 less the voltage drop across SCR3, with a positive polarity on its left terminal. Controlled rectifier SCR3 will continue to conduct minimum current through R2 and CR5. Controlled rectifier SCR4 will not conduct after its current becomes less than the minimum holding value.

After the prescribed time delay, as established by R12 and C6, controlled rectifiers SCR5 and SCR6 are gated on. Since the power contact SCR1-SCR2 is turned off, an auxiliary path consisting of resistors R8, 9, and 15 can discharge capacitor C5 through controlled rectifier SCR5. Because of the discharge path, SCR6 will not conduct, and SCR5 will cease conducting after C5 has been discharged.

To return the contactors to a conducting state, the turn-off signal is removed and the turn-on signal applied. With the turn-on signal applied, the dc control bus voltage is connected to C1-R2 and C5-R11 through diodes CR1 and CR5 and diodes CR3 and CR6 respectively. Turn off of SCR3 results because the instantaneous potential at its cathode becomes the sum of the control bus voltage and the voltage across C1. This reverse biases SCR3, turning

it off. Because of the time delay provided in the turn-on circuit by R22 and C11, capacitors C1 and C5 complete their charge with a positive polarity on the right terminal before gating signals become available for SCR1 and SCR2.

If the system voltage is such that controlled rectifier SCR1 is conducting instead of SCR2, application of the turn-off signal, after removal of the turn-on signal, will result in capacitor C1 discharging through SCR1. Resistor R5 is used to limit the magnitude of the discharge current. After the appropriate time delay provided by R22 and C11, capacitor C5 will discharge through SCR5 and SCR6, turning SCR1 off.

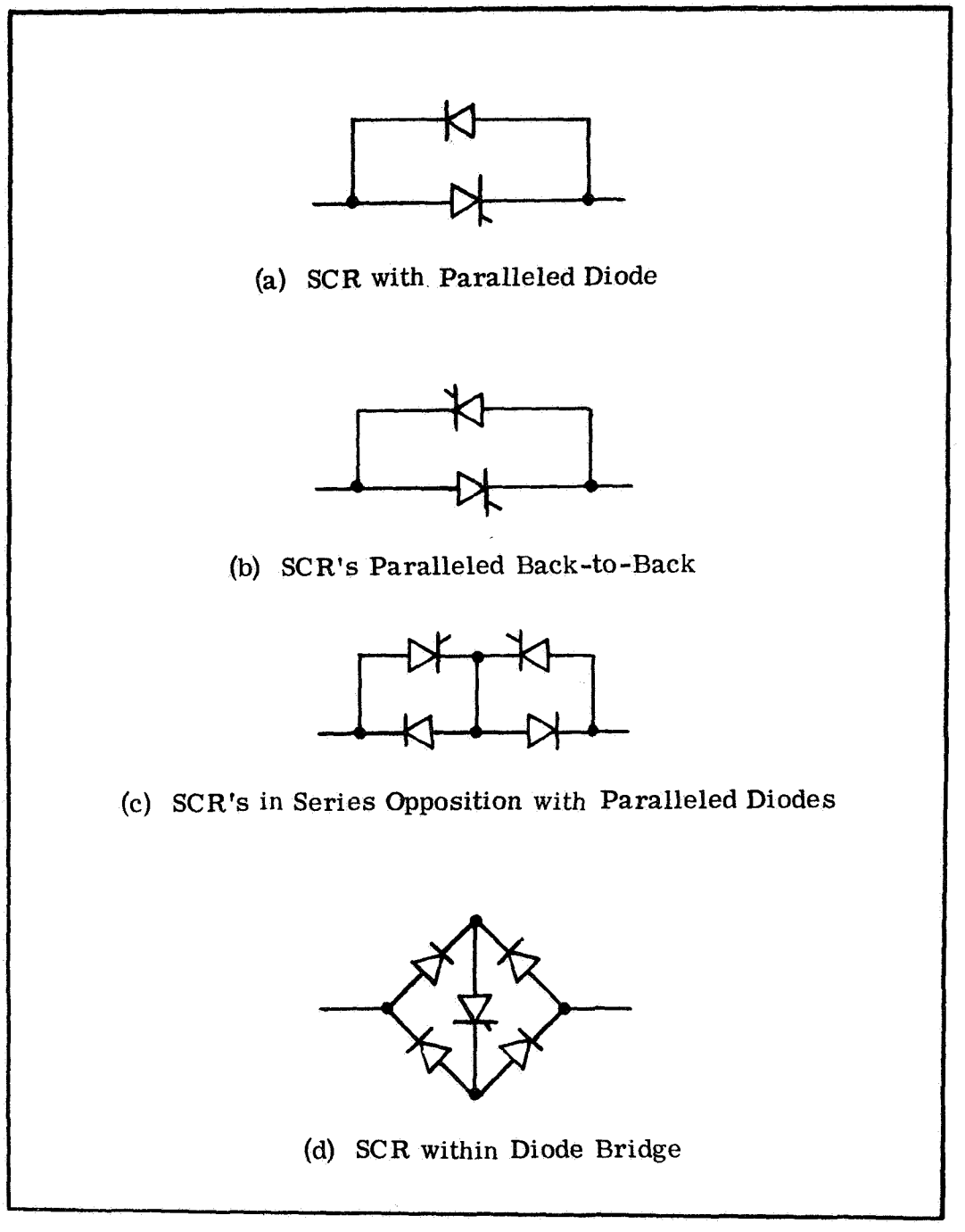
The estimated weight of only the electrical components for the circuit designs of figures 14 and 15 are 4.12 and 8.25 pounds respectively. These compare to a component weight of 3.02 pounds for the ICC/CCC of figure 12. The converter system LBC, LCC and TBC component weights are greater than those of the ICC/CCC because of the commutating capacitor. The use of an over-rated, standard, high voltage capacitor provides a voltage safety factor of approximately three rather than the desired factor of two. The commutating capacitor used for the LBC, LCC and TBC accounts for 90 percent of the electrical component weight.

The estimated efficiencies for the circuit designs of figures 14 and 15 are 99.2 percent as compared to the 96.9 percent obtained from test results for the ICC/CCC. This higher efficiency results because of the relatively lower voltage drop (on a percentage basis) for the controlled rectifiers of the LBC, LCC and TBC. As shown in table I, the operating voltage for the LBC, LCC and TBC is 153 ±5 volts as compared to the ICC/CCC voltage of 28 ±2 volts.

Inverter System Contactor Circuit Considerations

There are several possible power contact arrangements which can be used to make an alternating current static contactor with controlled rectifiers alone or in combination with diodes. Figure 16 illustrates these configurations showing a single-phase arrangement only for each representation.

The circuits of figure 16(a), (c), and (d) offer inverse voltage protection to the controlled rectifiers inherently through the use of diodes. In the forward direction voltage transients of sufficient magnitude could cause forward random or intermittent breakdown conduction unless adequately protected by auxiliary components or the controlled rectifiers are selected with forward voltage breakdown ratings in excess of the transients. Conversely, if the voltage and associated current transients are not in excess of the maximum SCR ratings, and if the load circuit can withstand the breakdown conduction transient, the controlled rectifiers will



(a) SCR with Paralleled Diode

(b) SCR's Paralleled Back-to-Back

(c) SCR's in Series Opposition with Paralleled Diodes

(d) SCR within Diode Bridge

Figure 16. - Controlled Rectifier AC Switching Circuits

not be damaged by this conduction and circuit operation should not be impaired. The disadvantage of the configurations of figure 16(c) and (d) is the multiple series forward voltage drop of the two and three semiconductor devices, respectively, with their associated power losses.

The circuit configuration of figure 16(a), although offering the advantage of reduced SCR gate control complexity, is not applicable to loads with a grounded neutral since half wave rectification would result. Therefore, the selected controlled rectifier contact arrangement is that of figure 16(b). With currently available, controlled rectifier reverse voltage ratings, inverse voltage transients should not be a problem with this selected circuit.

The use of controlled rectifiers in alternating current applications, unlike that of application in direct current circuits, does not require energy storage turn-off components. Controlled rectifiers used in an alternating current circuit will cease to conduct naturally on the first current zero after the removal of the gate-to-cathode signal. It therefore becomes necessary for the control circuit to provide a gate signal to the controlled rectifiers each time the alternating phase sequence provides a condition with the anode potential more positive than the cathode. To eliminate the possibility of phase control, it also becomes necessary for the gate signal to be available as soon as the anode polarity starts positive. This signal must be of sufficient duration to permit the anode current to become greater than the SCR holding current. This condition must be provided with inductive loads where the current lags its respective voltage.

Inverter System Contactor Designs

Inverter control contactor/converter control contactor. - The direct current ICC/CCC, which is common to the converter and inverter systems, was discussed previously.

Load bus, load control, and tie bus contactors. - The complete circuit diagram for the alternating current LBC, LCC and TBC is shown in figure 17. These contactors use the same electrical components since their power ratings are identical.

The power circuit static contacts, consisting of controlled rectifiers SCR1 through SCR6, are connected back-to-back in pairs, in series with the three power lines between the power source and the load. With the dc control bus energized with a potential of 22 to 30 volts, a regulated voltage of 15 volts is provided by resistor R31 and Zener diode CR21. This regulated voltage is applied to a Royer Oscillator. The controlled rectifier gate drives are supplied by this free running oscillator which provides

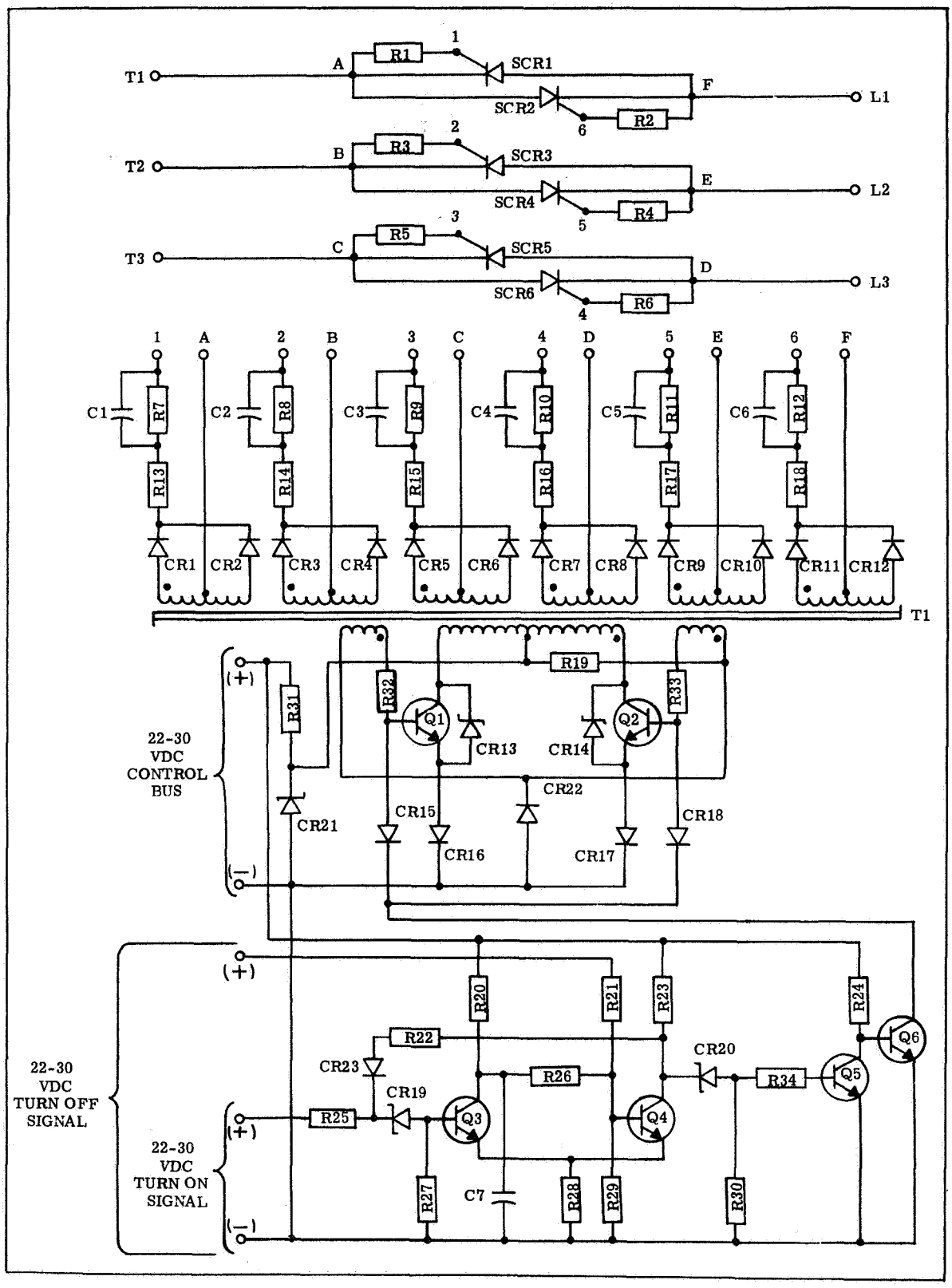


Figure 17. - Alternating Current Inverter System Static Contactor Circuit

electrical isolation between the contactor control and power circuits. The oscillator, which has been described in the literature, (ref. 5) is made up of transistors Q1 and Q2, saturating transformer T1, voltage spike suppression diodes CR13 and CR14, power transistor emitter circuit diodes CR15 and CR17, feedback winding diode CR22, feedback winding current limiting resistors R32 and R33, and starting resistor R19.

Isolated signals, resulting from the rectified oscillator square waves, gate the controlled rectifiers from six separate windings using rectifier diodes CR1 through CR12, current limiting resistors R7 through R18, and wave form shaping capacitors C1 through C6. With the oscillator running and line voltage applied, the static contactor will be closed. When the oscillator is shut down, gate signals are not provided to the controlled rectifiers SCR1 through SCR6; therefore, conduction ceases, line current is blocked, and the contactor is open.

The control logic for the contactors consists of a bistable Schmitt trigger which is composed of resistors R20, R23, R26, R28, and R29, capacitor C7 and transistors Q3 and Q4. When control bus voltage is first applied to the contactor, transistor Q4 conducts through resistors R23 and R28, after being forward biased from base to emitter by a voltage provided by resistors R20, R26, and R29. With Q4 on, transistor Q5 will be off, and transistor Q6 will be on. Transistor Q6 with diodes CR15 and CR18 short circuit CR16 and CR17 and the base to emitters of the oscillator transistors Q1 and Q2. This causes the oscillator to remain in a shutdown condition and consequently the contactor is open.

When a turn-on signal is applied, transistor Q3 is forward biased through resistors R25 and R27 and Zener diode CR19. With transistor Q3 conducting, Q4 is turned off. This results in Q5 turning on since it is forward biased through resistors R23 and R34 and Zener diode CR20; consequently, Q6 turns off causing the oscillator to run and the contactor to close. Since the turn-on signal is applied momentarily, feedback resistor R22 is provided to maintain transistor Q3 of the Schmitt trigger conducting. Diode CR23 isolates the turn-on signal from the collector of transistor Q4.

When a turn-off signal is applied, because of normal system shutdown or a system fault, transistor Q4 turns on after being forward biased through resistors R21 and R29. Transistor Q3 and Q5 will turn off and Q6 is turned on since it becomes forward biased from base to emitter through resistor R24. With Q6 conducting, oscillator operation ceases and the contactor is open. The contactor will remain opened until it is closed by a turn-on signal.

A photograph of the breadboard design of the inverter system LBC, LCC, and the TBC is shown in figure 18.

Figure 18. - Engineering Verification Model of Inverter System LBC, LCC, and TBC

The estimated weight of only the electrical components for the LBC, LCC and TBC contactors is 1.04 pounds.

Experimental Evaluation of Static Contactor Designs

Experimental test results of the static designs of the ICC/CCC and the inverter system LBC, LCC and TBC are reported in this section. The static contactors were conencted into a power source and load circuit and the evaluation tests performed.

For purposes of clarity and expendiency in performing the tests in the laboratory, the different types of load tests such as resistive, inductive-resistive, and capacitive-resistive, as applicable, were performed separately on each of the two contactor designs. The reporting of the results of these tests, however, is accomplished according to the magnitude of the applied load current which includes all of the load types applied to each specific contactor design. This, it is believed, permits less repetition in the reporting of the acquired results and provides for a direct comparison of the measured data.

Test results of ICC/CCC design. - The two types of dc loads applied to the ICC/CCC were resistance and inductive-resistive. An inductance-to-resistance load ratio of 0.0011 at one per unit rated current and one per unit rated voltage was used for the resistive-inductive load test. Figure 19 shows the laboratory test circuit used to evaluate the ICC/CCC static contactor.

During the testing of the direct current ICC/CCC, a change was made in the controlled rectifier power contact SCR1. This was done when the initial controlled rectifier did not turn off when subjected to inductive-resistive load currents of 200 and 250 percent of rated load. The SCR1 power contact was changed from a 110-ampere, rms device to a 235-ampere, rms device.

No-load measurements: The results of this test show that the leakage current through SCR1 was 26 microamperes with the contactor "opened", with the power contact SCR1 case temperature at room ambient, and with 28 volts dc applied to the input terminals T1-T2. With the contactor "opened", immediately after temperature stabilization[1] of SCR1 at a one per unit current of 40 amperes, the leakage current through SCR1 was 48 microamperes. Because the temperature of SCR1 decreases very rapidly after removal of load current, the difference between the stabilized case temperature of SCR1 with load current and when the leakage current of 48 microamperes was measured was 40°F.

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[1]Temperature stabilization is that point when a thermocouple attached to the case of the SCR attains a steady-state value.

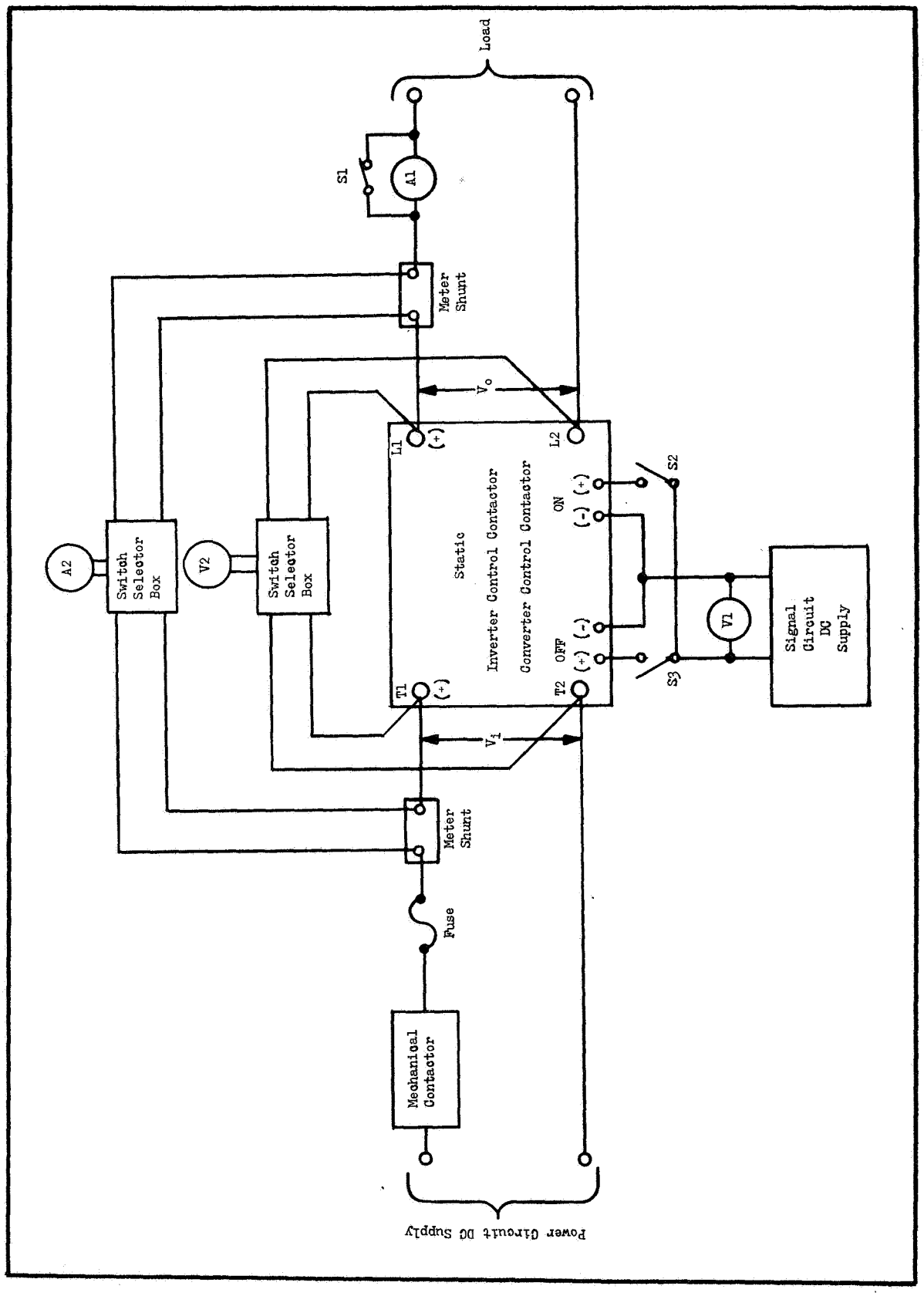


Figure 19. - Static ICC/CCC Test Circuit

Rated-load measurements: With the load current adjusted to 40 amperes and the voltage across the contactor output terminals L1-L2 at 28 volts dc, measurements of contactor input and output voltage and current were recorded before and after the case temperature of SCR1 was stabilized. The contactor efficiency, at rated current of 40 amperes, is 96.2 percent with the 110-ampere controlled rectifier and 96.94 percent with the 235-ampere controlled rectifier. The increased efficiency results because of a lower forward voltage drop. The voltage drop of 0.88 volts dc across the 235-ampere-controlled rectifier at a stabilized case temperature rise of 76°F compares to a voltage drop of 1.115 volts dc with the 110-ampere controlled rectifier at a stabilized case temperature rise of 97°F.

After the case of SCR1 was temperature stabilized at a 40-ampere resistive and 40-ampere inductive-resistive load, oscillograms of load application and load removal were taken. Figures 20 and 21 are the oscillograms of load current application from zero to 40 amperes and load removal from 40 amperes to zero for a resistive load. Figure 22 presents the same load current switching for an inductive-resistive load. From the oscillograph traces of contactor output voltage (Vo) and contactor output current (SCR1 current) it is seen that output voltage and current are delivered to the load with the application of a turn-on signal and that the output voltage and current are removed from the load with application of a turn-off signal. Therefore, it is seen that the basic requirement of contactor operation, which is the conduction and interruption of a load current, is satisfactory. The delay of approximately 0.07 seconds between the time of signal application and until load current flows is the intentional time delay designed into the control circuit to permit capacitor C1 to acquire full voltage prior to controlled rectifier SCR1 turning on.

Figure 23 shows oscilloscope pictures of the transient current through and the voltage across the power contact SCR1 with resistive and inductive-resistive load application from zero to 40 amperes after the case of SCR1 was temperature stabilized at the contactor one per unit current rating of 40 amperes.

Overload measurements: The purpose of this test was to subject the ICC/CCC to a 125 percent load (50 amperes) for five minutes and to discern and record operation. The specified load current and time limit are overload requirements for the existing inverter/converter.

This test was performed by temperature stabilizing the case of SCR1 with a 40-ampere resistive load. The load current was then increased to 50 amperes and retained at this value for five minutes. Contactor input and output voltages and currents were recorded after temperature stabilization of SCR1 and at the beginning and end of the five-minute period. The measured power con-

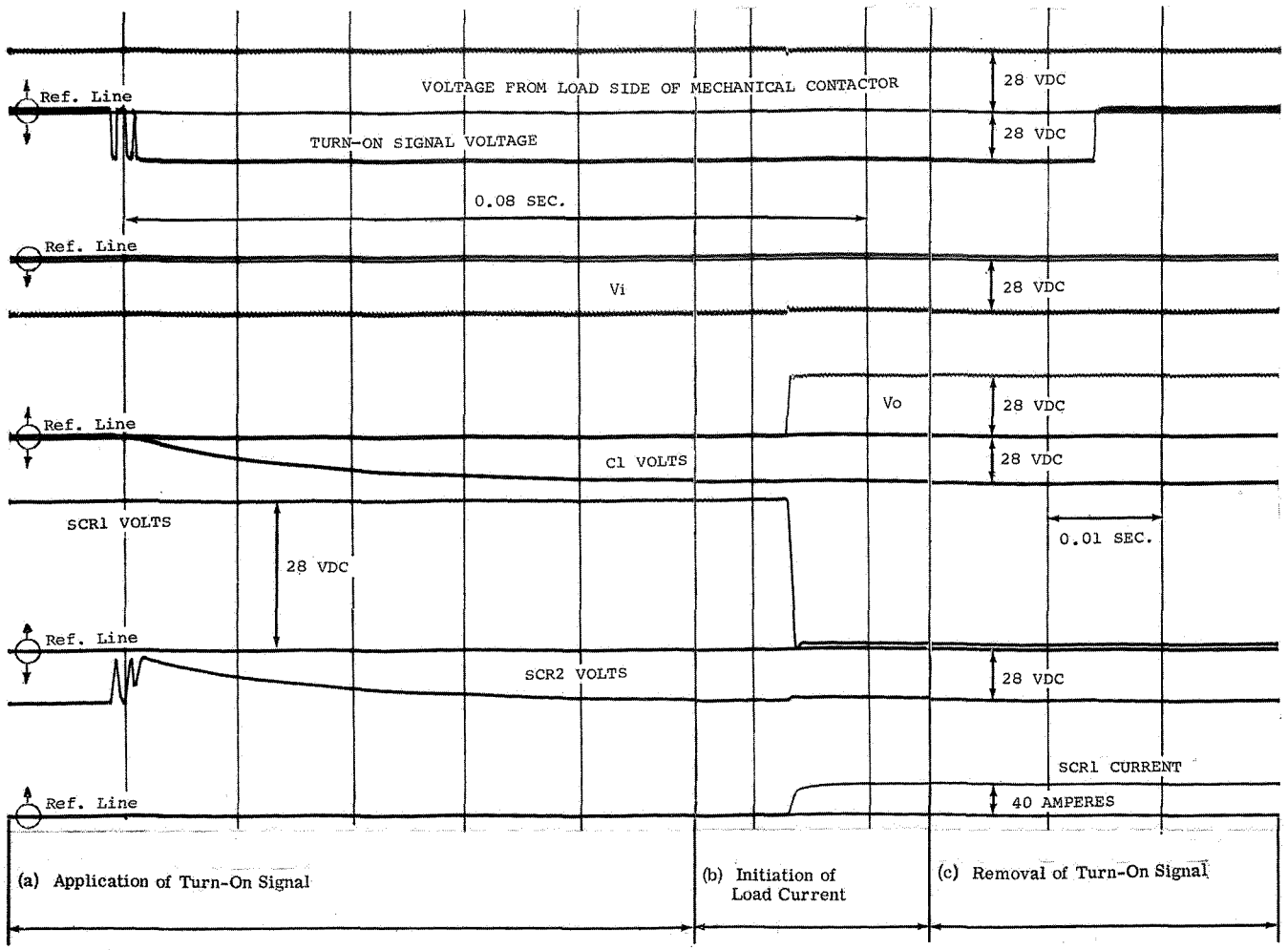


Figure 20. - Static Converter Control Contactor Oscillogram of Resistive Load, Line Current 0 to 40 to 0 Amperes

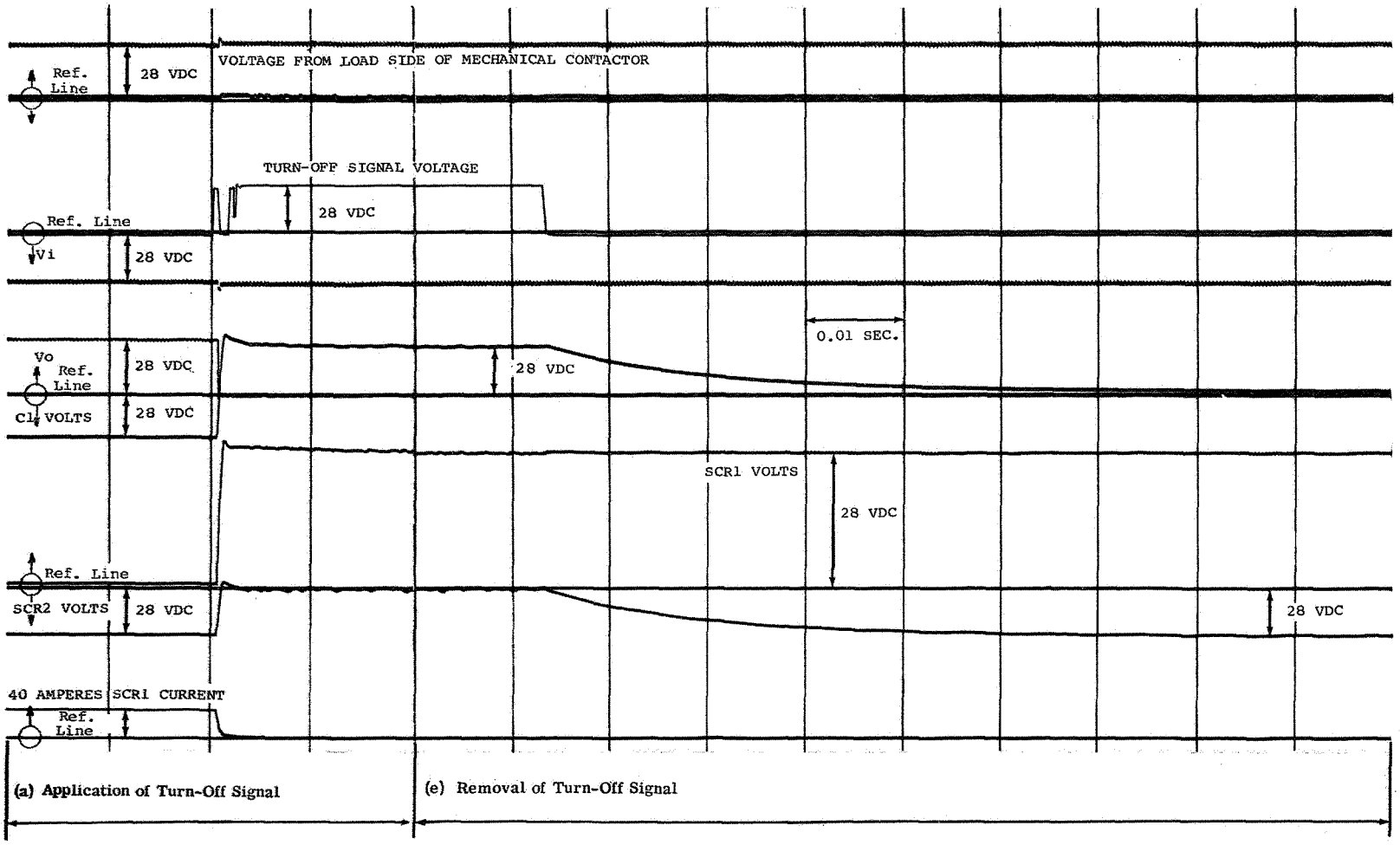


Figure 21. - Static Converter Control Contactor Oscillogram of Resistive Load, Line Current 0 to 40 to 0 Amperes

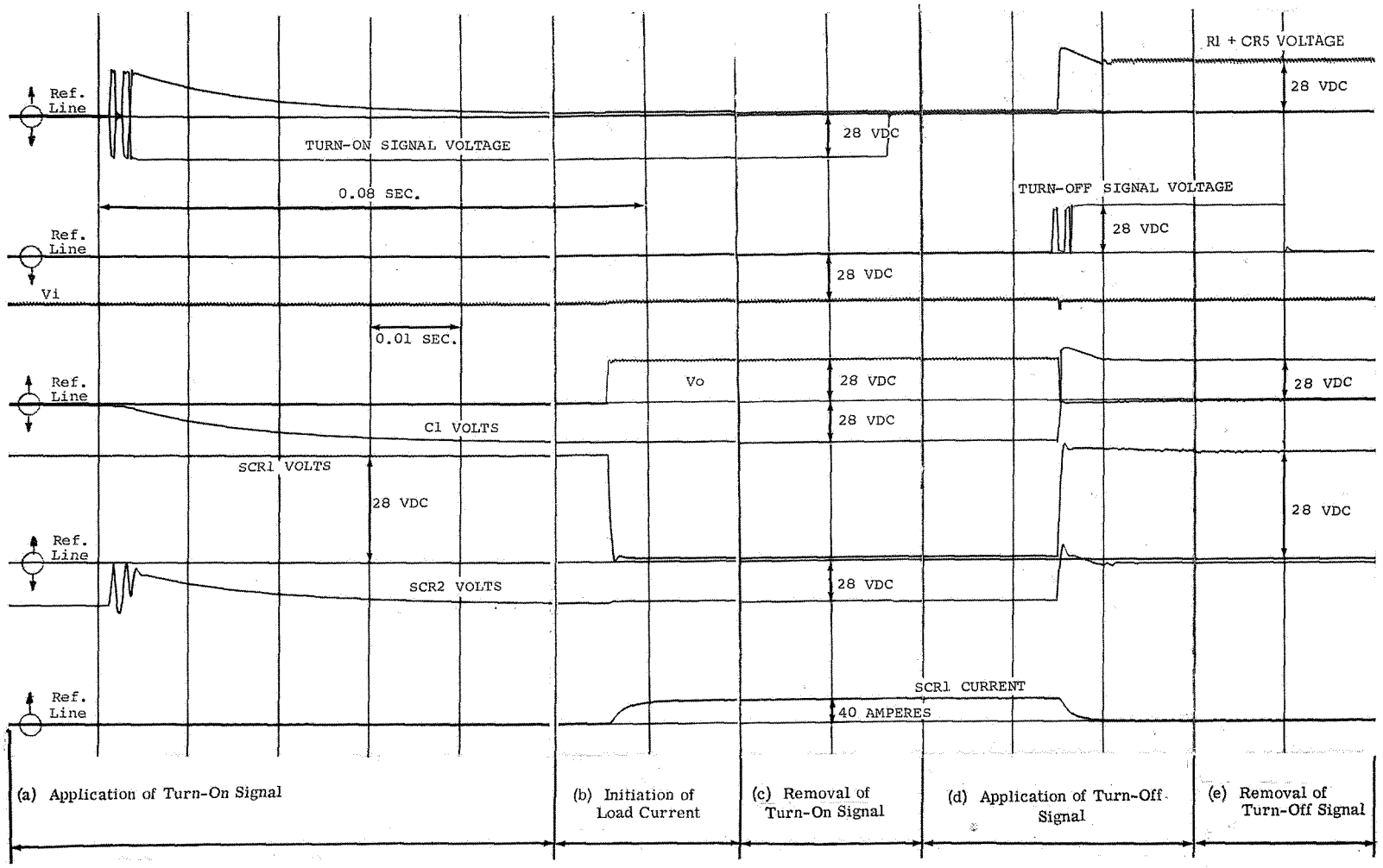
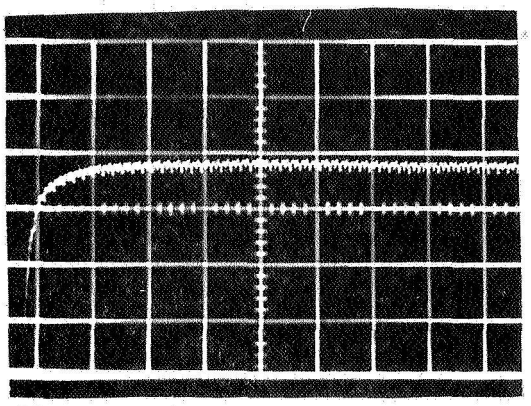
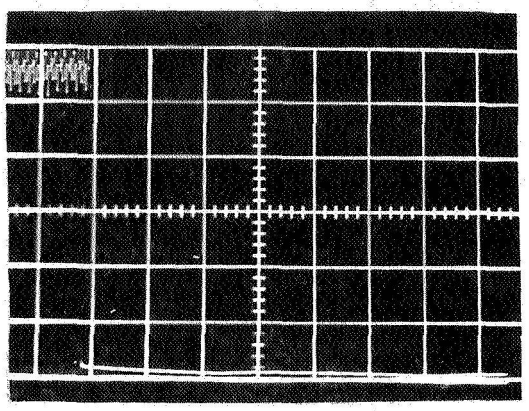


Figure 22. - Static Converter Control Contactor Oscillogram of Inductive-Resistive Load, Line Current 0 to 40 to 0 Amperes



10 AMPERES PER DIVISION, VERTICAL
2 MILLISECONDS PER DIVISION, HORIZONTAL

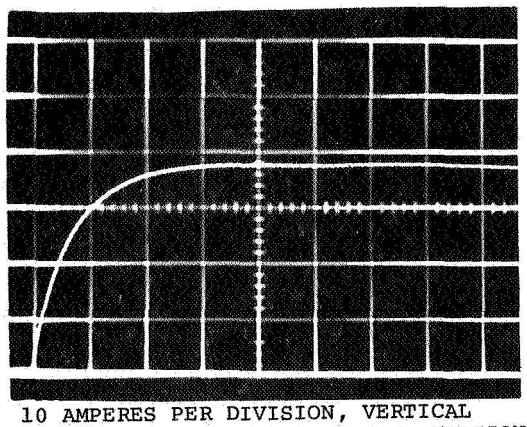
CURRENT TRANSIENT



5 VOLTS PER DIVISION, VERTICAL
2 MILLISECONDS PER DIVISION, HORIZONTAL

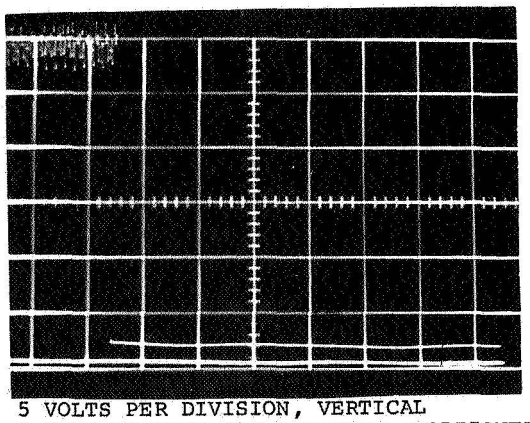
VOLTAGE TRANSIENT

0 to 40 Amperes, Resistive Load



10 AMPERES PER DIVISION, VERTICAL
2 MILLISECONDS PER DIVISION, HORIZONTAL

CURRENT TRANSIENT



5 VOLTS PER DIVISION, VERTICAL
2 MILLISECONDS PER DIVISION, HORIZONTAL

VOLTAGE TRANSIENT

0 to 40 Amperes, Inductive-Resistive Load

Figure 23. - Static ICC/CCC Voltage and Current Transients of Power Contact, SCR1, During Load Application

tact SCR1 case temperature increased by 20°F from a stabilized temperature rise of 96°F during the five-minute, 50-ampere load application. The recorded voltage drop across SCR1 remained unchanged for the load currents of 40 and 50 amperes. With the conduction and interruption of a 50-ampere load performed without exceeding the temperature rating of SCR1, it is concluded that contactor operation for a 125 percent load is satisfactory.

Overload application and removal: After the case of SCR1 was temperature stabilized at a 40-ampere resistive and 40-ampere inductive-resistive load, an oscillogram was taken of current increase to 80 amperes and load removal. Figures 24 and 25 are the oscillograms of load current increase from 40 to 80 amperes and load removal from 80 amperes to zero for the resistive and inductive-resistive loads, respectively. The static contactor interrupted the 80-ampere load one second after application with a mechanical contactor, used as a back-up device, operating 200 milliseconds later. The reason for the interruption of a smooth current build-up for the SCR1 current trace to 80 amperes from the ititial 40-ampere level has not been investigated. This affect may be caused by a momentary lack of a sufficient number of carriers in SCR1.

Figure 26 shows oscilloscope pictures of the transient current through and the voltage across the power contact SCR1 with resistive and inductive-resistive load current increase from 40 to 80 amperes after the case of SCR1 was initially temperature stabilized at the 40-ampere load.

Short circuit application and removal: Using the same test procedure described for the 200-percent loads, short-circuit current oscillograms and oscilloscope pictures were taken. Figures 27 and 28 are the oscillograms of load current increase from 40 to 100 amperes and load removal from 100 amperes to zero for the resistive and inductive-resistive loads, respectively. The static contactor interrupted the 100-ampere short-circuit current 800 milliseconds after application with the mechanical contactor, used for back-up, operating 200 milliseconds later.

The oscilloscope pictures of transient current through and the voltage drop across SCR1 with resistive and inductive-resistive load current increase from 40 to 100 amperes, after the case of SCR1 was temperature stabilized at the 40 ampere load, are shown in figure 29.

Cycling: With a resistive load adjusted to 40 amperes and the voltage across the contactor output terminals L1 and L2 at approximately 28 volts, the case of SCR1 was temperature stabilized. Contactor output and input voltages and currents were recorded before and after temperature stabilization of SCR1. After temperature stabilization the contactor was satisfactorily cycled on and off

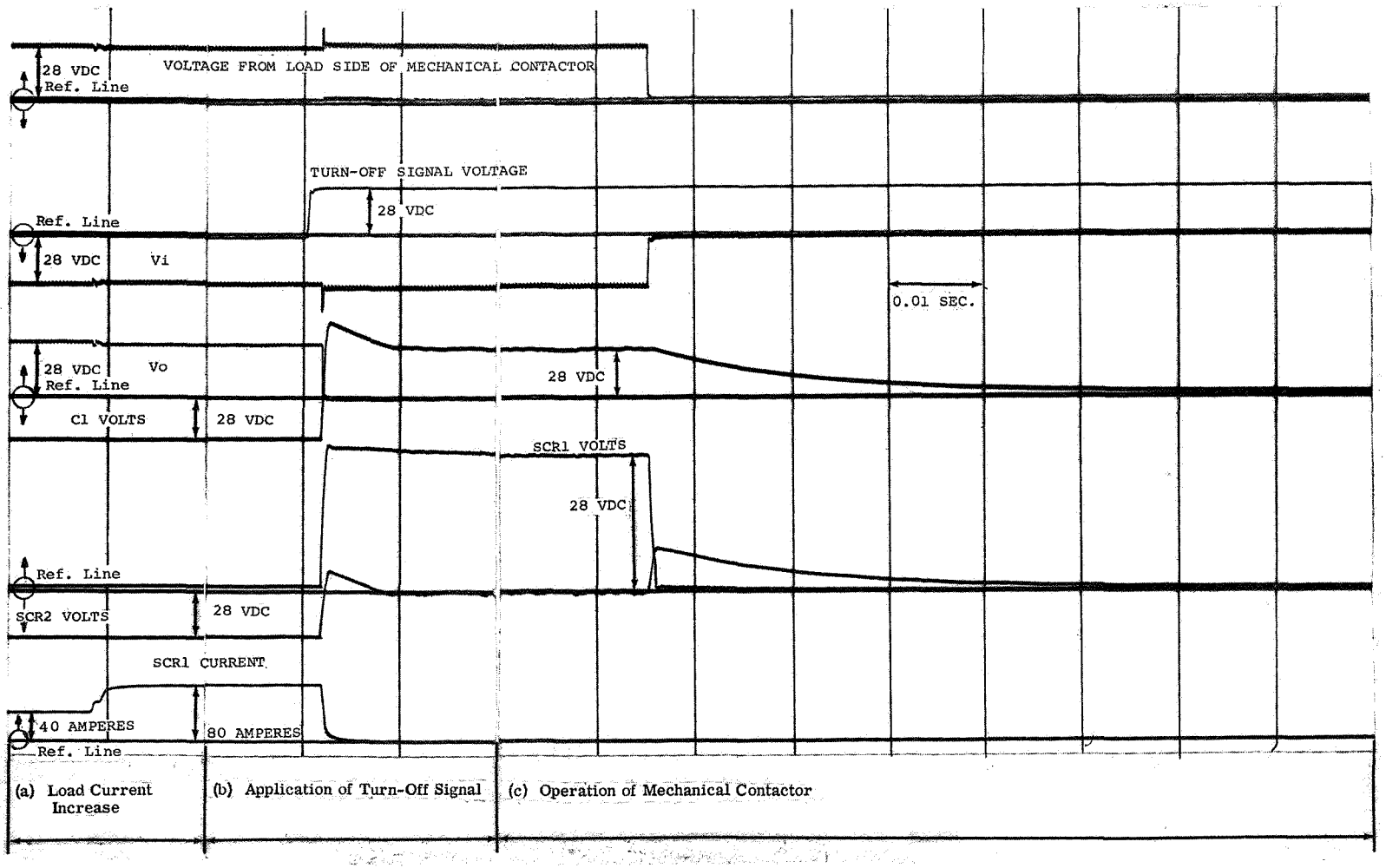


Figure 24. - Static Converter Control Contactor Oscillogram of Resistive Load, Line Current 40 to 80 to 0 Amperes

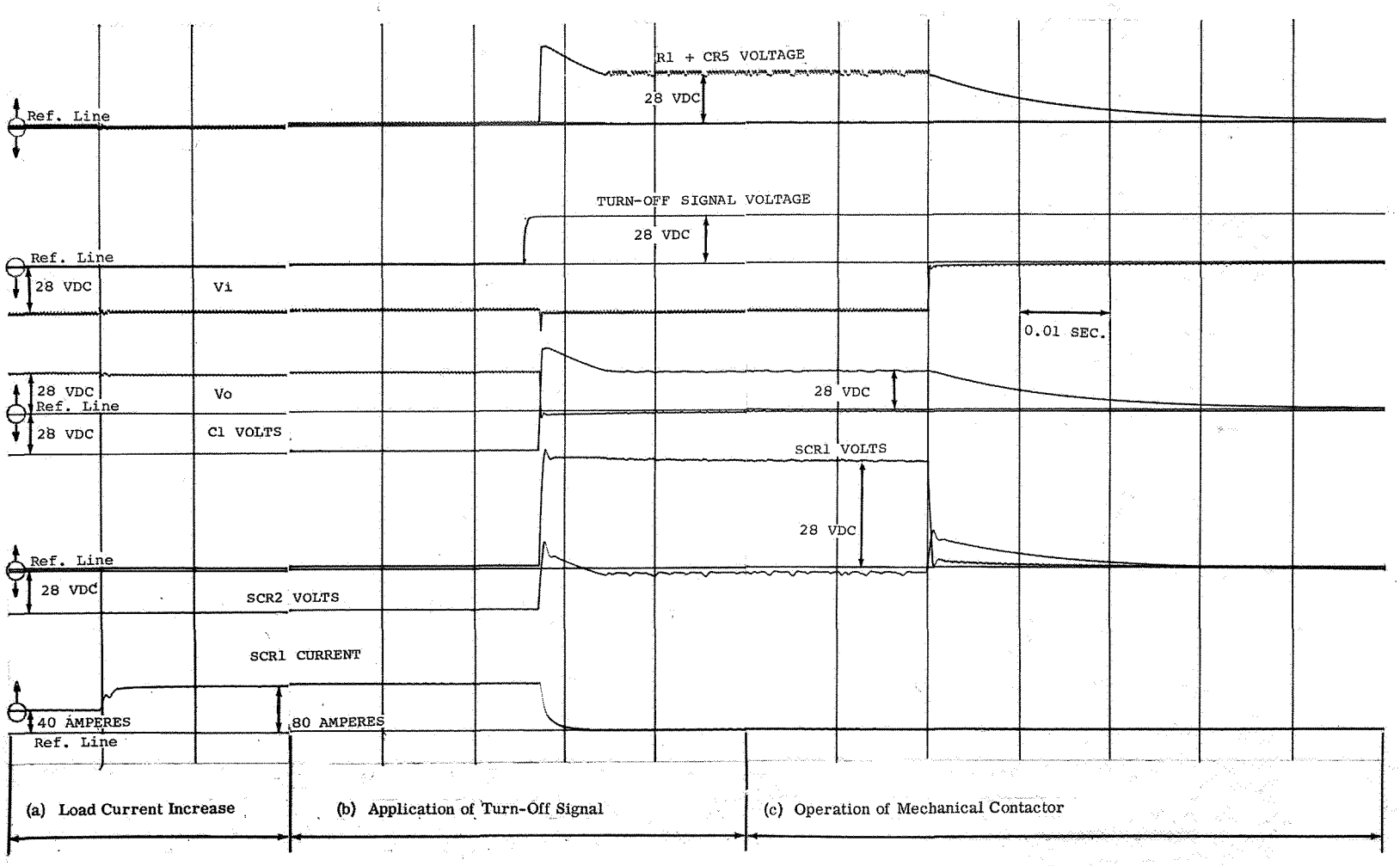
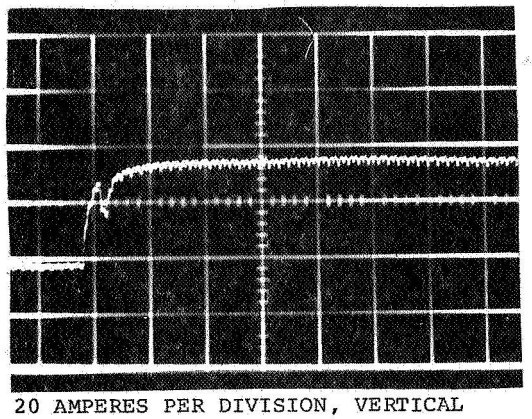
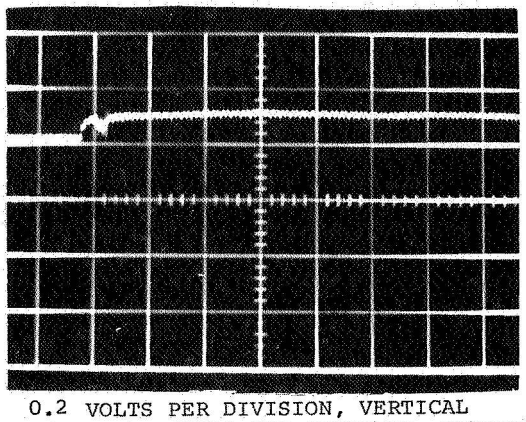


Figure 25. - Static Converter Control Contactor Oscillogram of Inductive-Resistive Load, Line Current 40 to 80 to 0 Amperes



20 AMPERES PER DIVISION, VERTICAL
2 MILLISECONDS PER DIVISION, HORIZONTAL

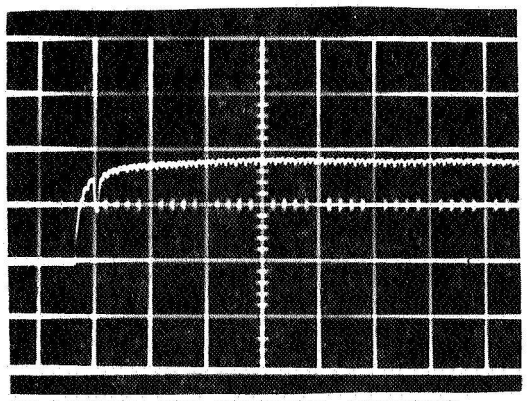
CURRENT TRANSIENT



0.2 VOLTS PER DIVISION, VERTICAL
2 MILLISECONDS PER DIVISION, HORIZONTAL

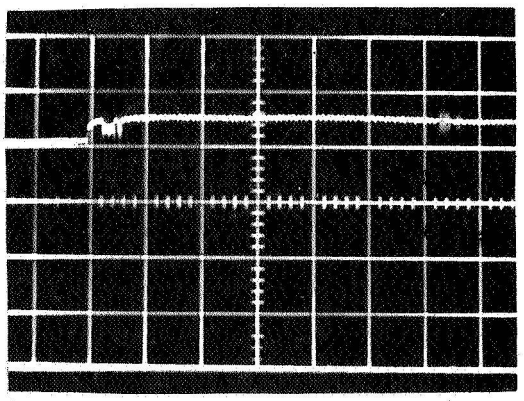
VOLTAGE TRANSIENT

40 to 80 Amperes, Resistive Load



20 AMPERES PER DIVISION, VERTICAL
2 MILLISECONDS PER DIVISION, HORIZONTAL

CURRENT TRANSIENT



0.2 VOLTS PER DIVISION, VERTICAL
2 MILLISECONDS PER DIVISION, HORIZONTAL

VOLTAGE TRANSIENT

40 to 80 Amperes, Inductive-Resistive Load

Figure 26. - Static ICC/CCC Voltage and Current Transients of Power Contact, SCR1, During Load Increase

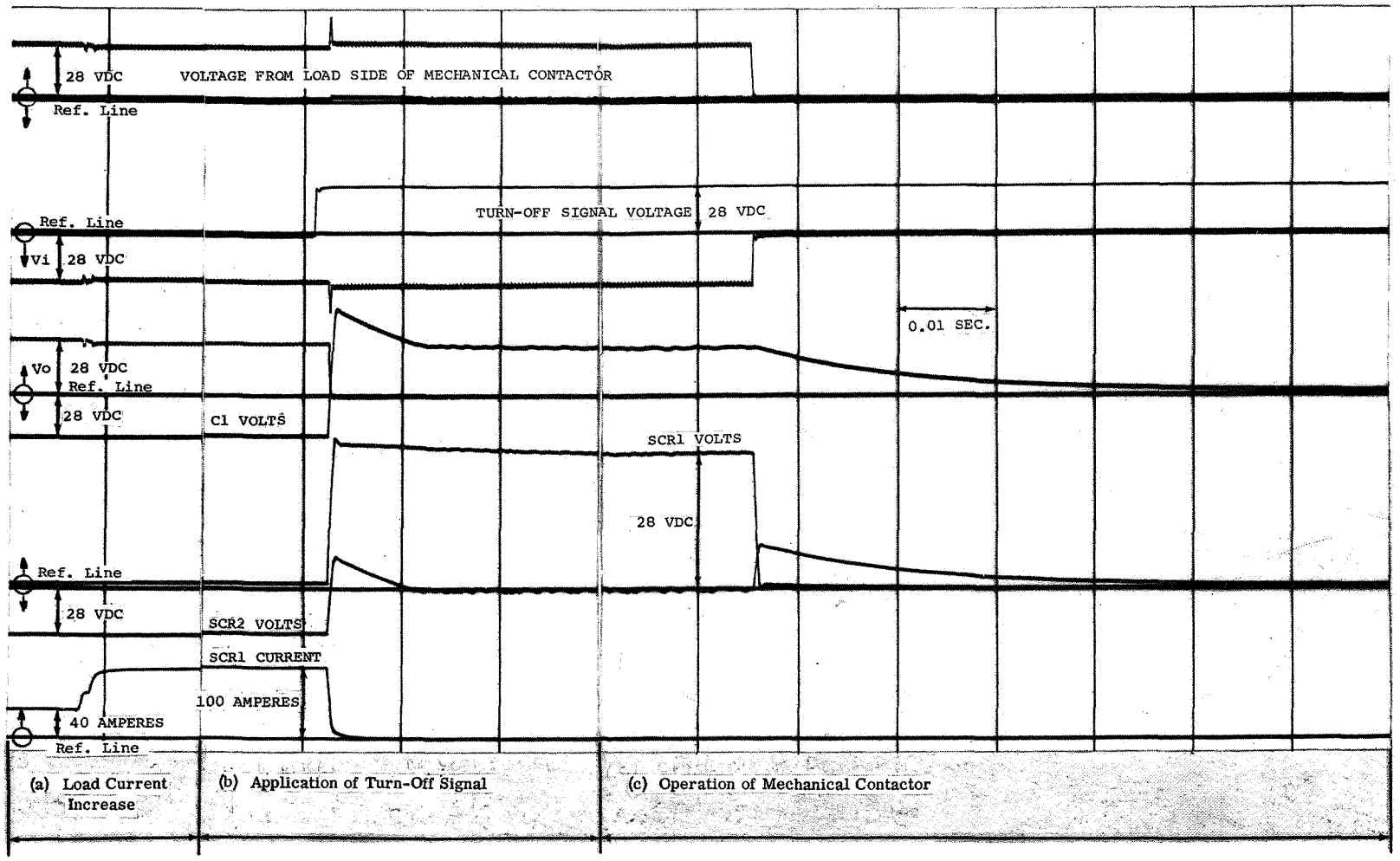


Figure 27. - Static Converter Control Contactor Oscillogram of Resistive Load, Line Current 40 to 100 to 0 Amperes

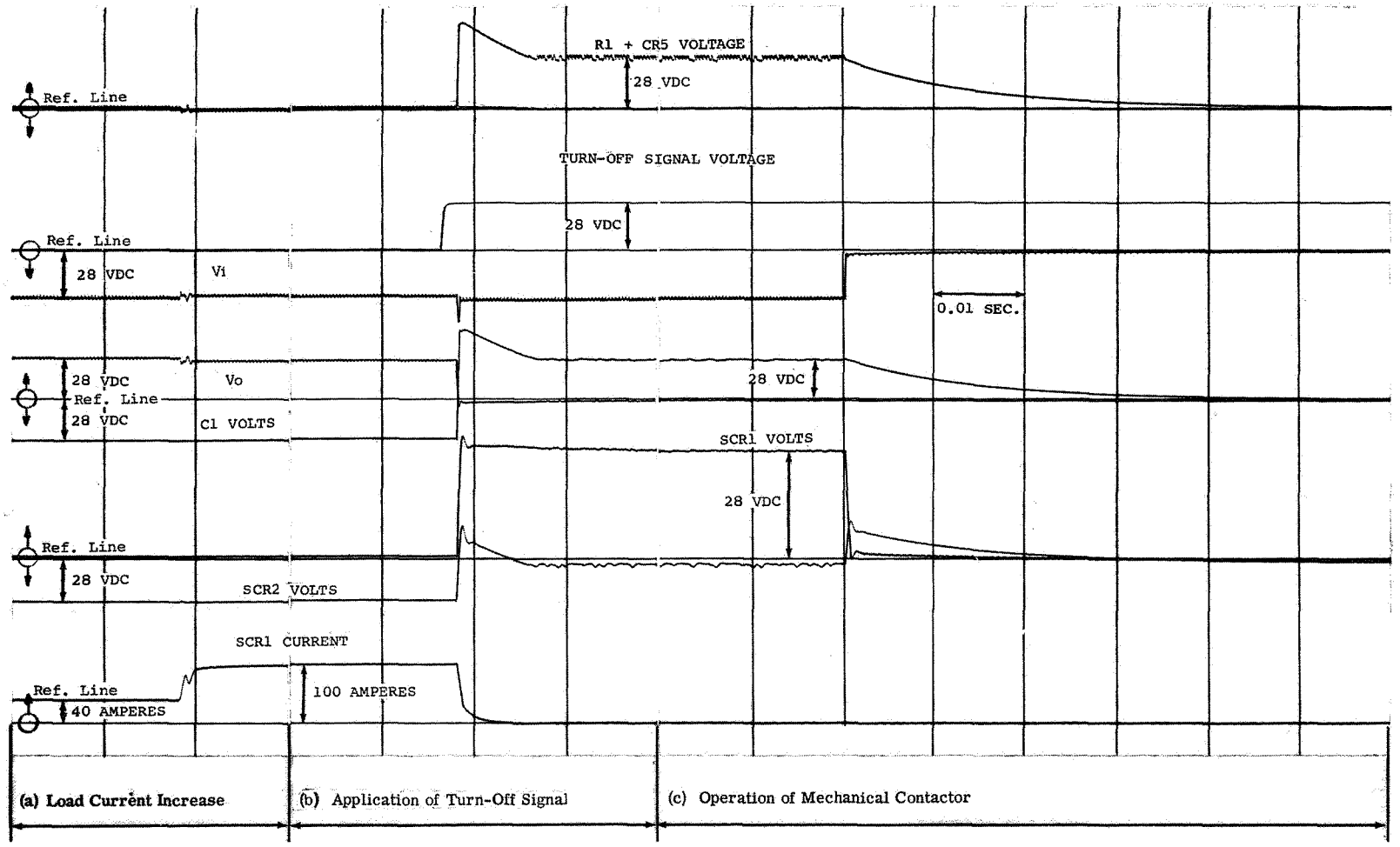
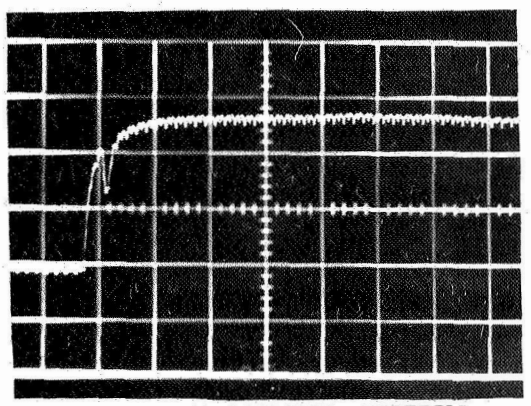
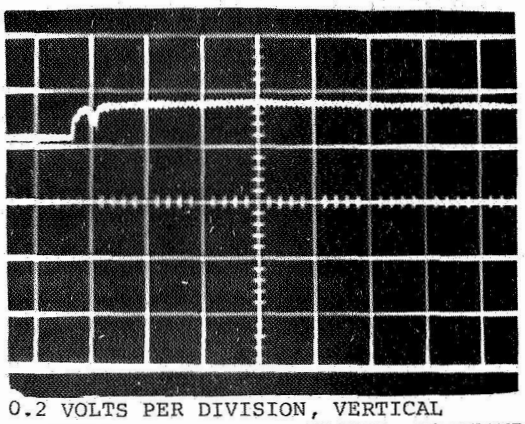


Figure 28. - Static Converter Control Contactor Oscillogram of Inductive-Resistive Load, Line Current 40 to 100 to 0 Amperes



20 AMPERES PER DIVISION, VERTICAL
2 MILLISECONDS PER DIVISION, HORIZONTAL

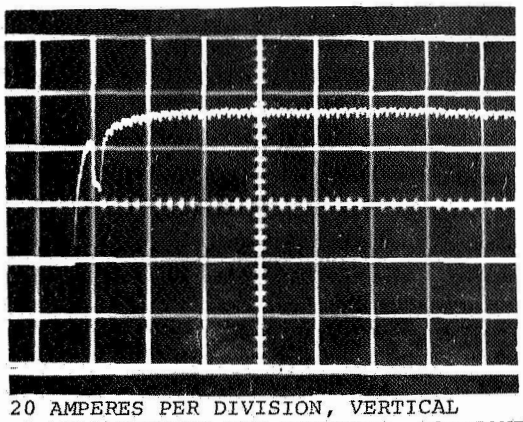
CURRENT TRANSIENT



0.2 VOLTS PER DIVISION, VERTICAL
2 MILLISECONDS PER DIVISION, HORIZONTAL

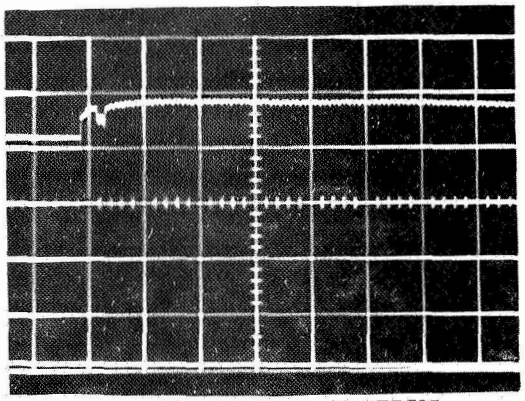
VOLTAGE TRANSIENT

40 to 100 Amperes, Resistive Load



20 AMPERES PER DIVISION, VERTICAL
2 MILLISECONDS PER DIVISION, HORIZONTAL

CURRENT TRANSIENT



0.2 VOLTS PER DIVISION, VERTICAL
2 MILLISECONDS PER DIVISION, HORIZONTAL

VOLTAGE TRANSIENT

40 to 100 Amperes, Inductive-Resistive Load

Figure 29. - Static ICC/CCC Voltage and Current Transients of Power Contact, SCR1, During Load Increase

for a total of 50 cycles such that the contactor was on for 10 seconds and off for 0.25 seconds.

Test results of inverter system LBC, LCC and TBC design. - Three types of ac loads were applied to the inverter system contactor which is capable of functioning as the LBC, LCC and TBC. These loads were resistive, inductive-resistive at 0.75 lagging power factor, and capacitive-resistive at 0.75 leading power factor. Figure 30 shows the laboratory test circuit used to evaluate the ac static contactors.

After the completion of the resistive and 0.75 leading power factor load tests, a resistive-capacitive network was applied line-to-line across the output terminals of the static contactor prior to performing the 0.75 lagging power factor load tests. The network consisted of a 10-ohm, 2-watt, wire-wound resistor in series with the equivalent of a 0.23-microfarad, 1000-volt capacitor. This network was used on the static contactor, as a precautionary measure, to suppress any voltage spikes which might result because of current interruption of an inductive load. This action was undertaken when consideration was initially given to the possible reasons the direct current ICC/CCC failed to interrupt the 200 and 250 percent inductive-resistive load currents. Upon reconsideration of the method of turning off the inverter system controlled rectifier contactor, it is realized that inductive voltage spikes cannot be generated since the controlled rectifier as applied in the alternating current circuit will cease to conduct on the first current zero after removal of the gating signal. This is verified in the oscillogram traces. Therefore, at contactor turn off, energy is not stored in the load inductor since the current through it has been reduced to zero and then extinguished.

No-load measurements: The purpose of the no-load tests was to record information on the contactor no-load performance.

Control circuit voltage and current measurements were made to be able to determine total contactor efficiency under load. The steady state control requirement with the off signal energized is 0.82 amperes at 28 volts dc. With the on signal energized, the control requirement is 0.845 amperes at 28 volts dc. The on and off signal voltage and current requirements will not enter into the efficiency calculations because they are only applied momentarily.

With the static contactor "opened" and the three-phase voltage at the input terminals T1-T2-T3 at 200 volts, rms, line-to-line, at 400 cycles per second, the average voltage across the three-power contact was 112.6 volts, rms. The leakage current of the controlled rectifier power contacts could not be read and was recorded at zero. This result was recorded with the controlled rectifier case temperatures at room ambient and immediately after

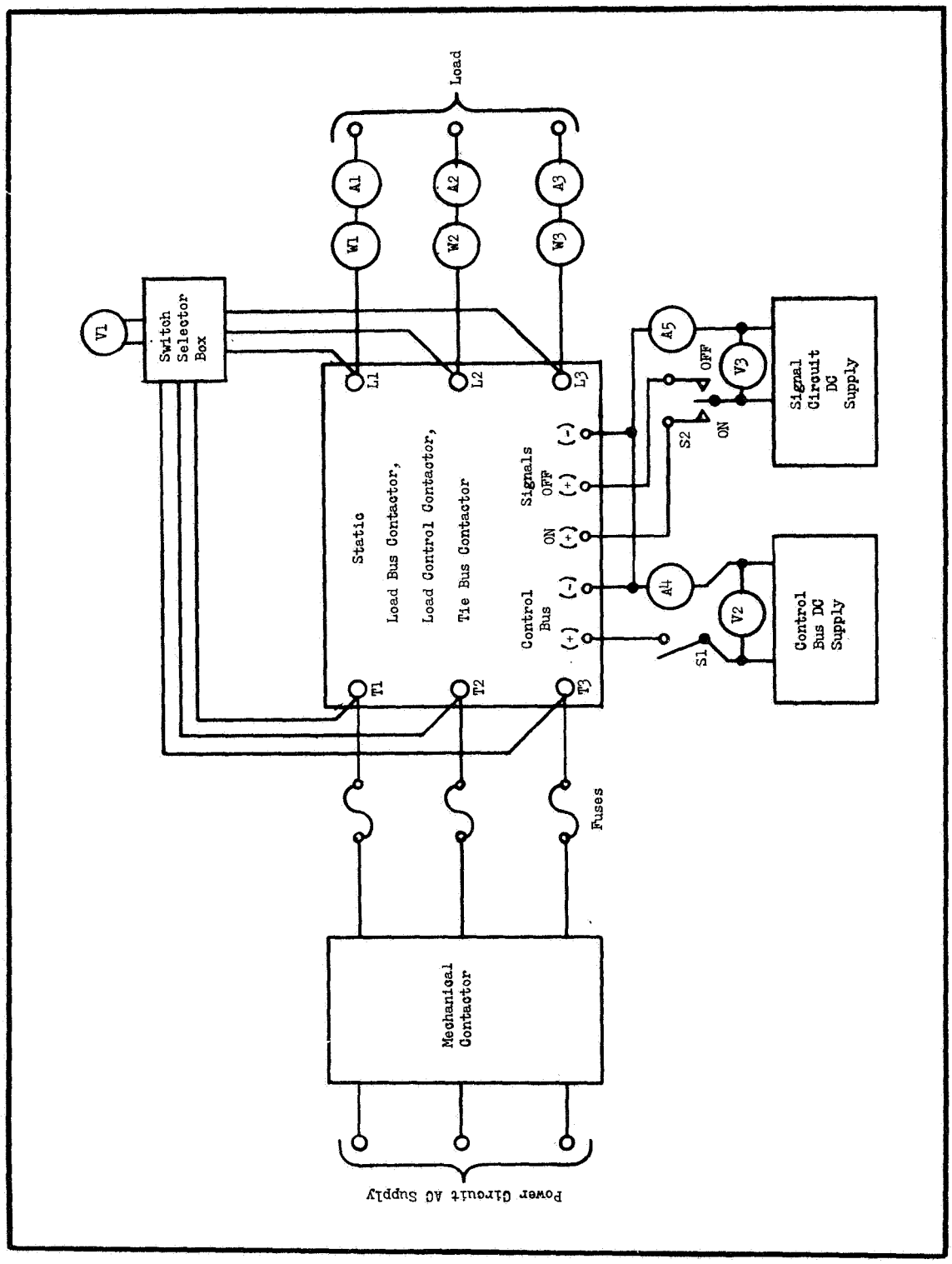


Figure 30. - Static LBC, LCC, and TBC Test Set Up

being temperature stabilized at the one per unit contactor current rating of 2.2 amperes, rms. Controlled rectifiers SCR1, SCR3, and SCR5 were temperature monitored.

Rated-load measurements: With the three-phase, balanced, wye-connected load adjusted to 2.2 amperes, rms per phase and the voltage across the contactor output terminals L1 and L2, L2 and L3, and L1 and L3 at 200 volts, rms, measurements of contactor input and output voltage, current, and wattage were recorded after the case temperatures of SCR1, SCR3, and SCR5 were stabilized. The average voltage drop of all three power contacts, measured with an oscilloscope, was 1.315 volts rms at a one per unit current rating of 2.2 amperes, rms resistive. The stabilized temperature rise was 15° to 19°F above the reference temperature of 75°F. The contactor efficiency at 2.2 amperes rms resistive per phase, including the power loss of the control circuit, is 95.9 percent.

After case temperature stabilization of controlled rectifiers SCR1, SCR3, and SCR5 with a three-phase balanced load of 2.2 amperes, rms resistive, capacitive-resistive and inductive-resistive, oscillograms of load application and load removal were taken. Figures 31, 32 and 33 are the oscillograms of load current application from zero to 2.2 amperes and load removal from 2.2 amperes to zero for the resistive, capacitive-resistive, and inductive-resistive loads, respectively. From the oscillograph traces of contactor output voltage (L1-L2 and L2-L3) and contactor output current (L1, L2, and L3), it is seen that output voltage and current are delivered to the load with the application of a turn-on signal and that the output voltage and current are removed from the load with application of a turn-off signal. Since this fulfills the basic requirement of power contactor, it is concluded that the static contactor performed satisfactorily.

Figures 34 and 35 show oscilloscope pictures of the transient current through the voltage across the power contact of SCR1 and SCR2 with resistive, inductive-resistive and capacitive-resistive load application from zero to 2.2 amperes, rms after the case temperature of SCR1 was stabilized at 2.2 amperes. The unsymmetrical voltage drop across the controlled rectifiers, about the zero reference line, is a result of the current probe in series with the cathode of the controlled rectifier. Because the current and voltage transient photographs were not taken simultaneously, direct comparisons cannot be made.

Overload measurements: The purpose of this test was to subject the inverter system LBC, LCC, and TBC to a 125 percent load (2.75 amperes) for five minutes and to discern and record operation. Contactor operation for this condition was satisfactory.

This test was performed by temperature stabilizing the cases of controlled rectifiers SCR1, SCR3, and SCR5 with a three-phase,

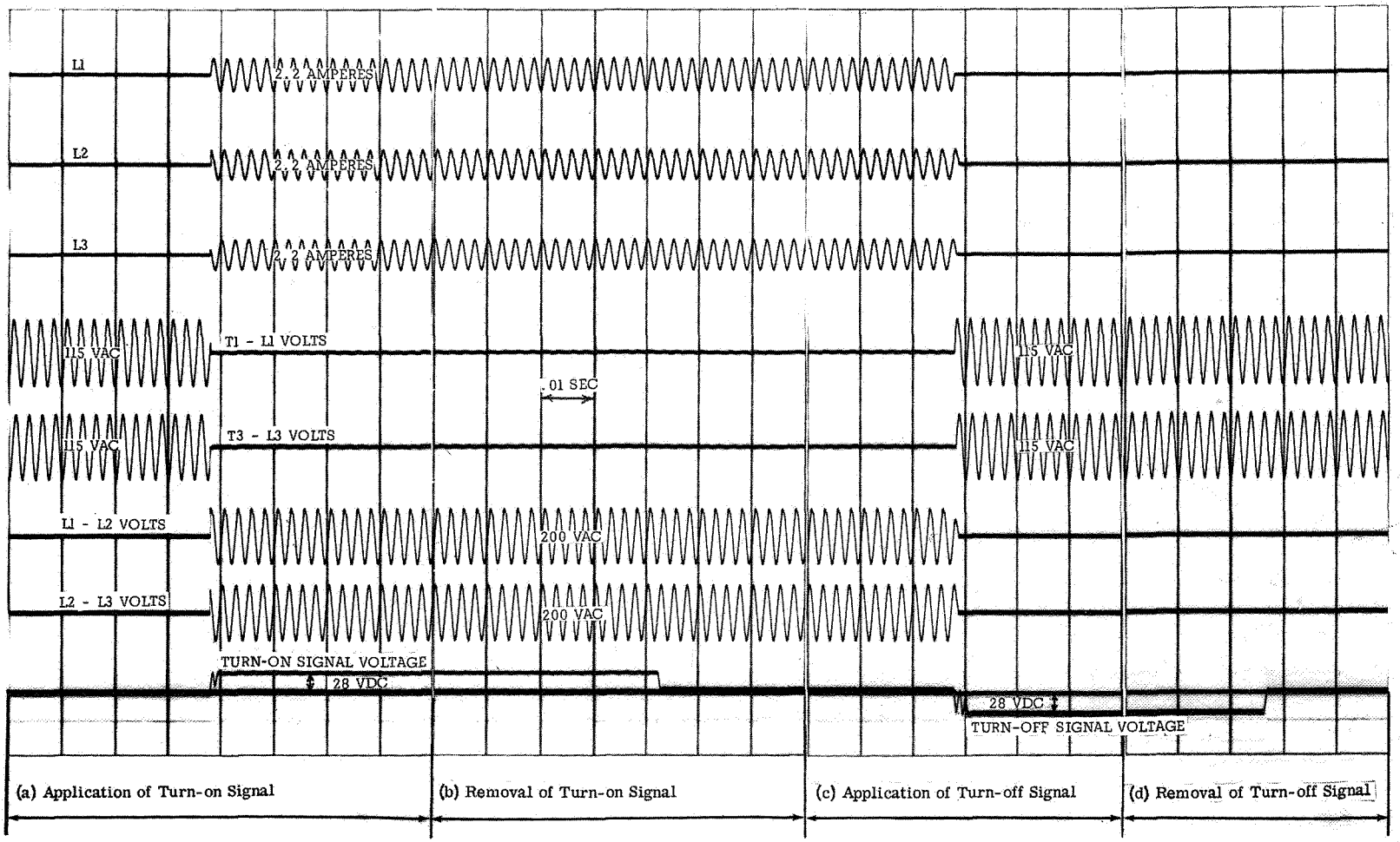


Figure 31. - Inverter System Static Contactor Oscillogram of Resistive Load, Line Current 0 to 2.2 to 0 Amperes

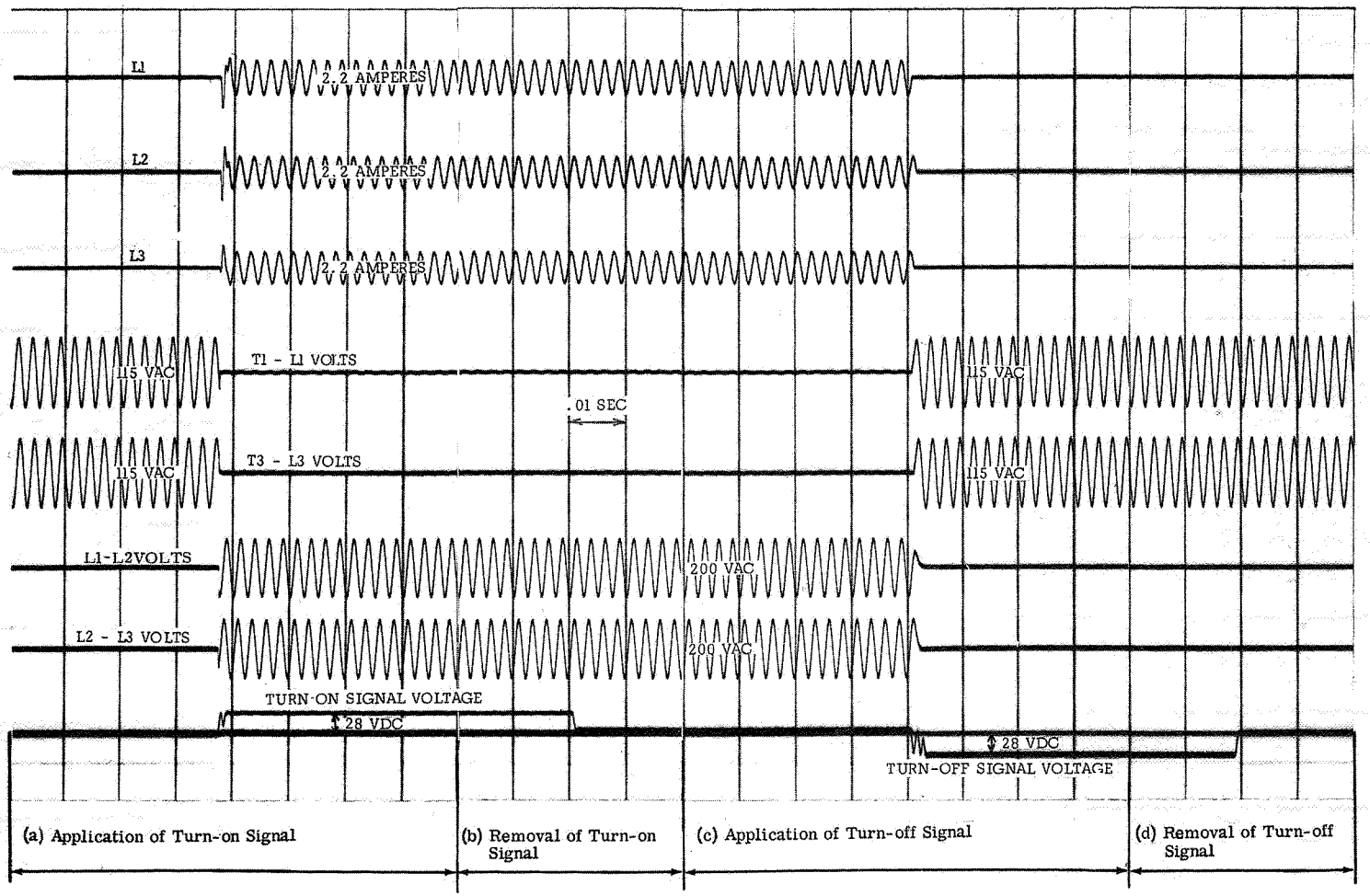


Figure 32. - Inverter System Static Contactor Oscillogram of Capacitive-Resistive Load, Line Current 0 to 2.2 to 0 Amperes

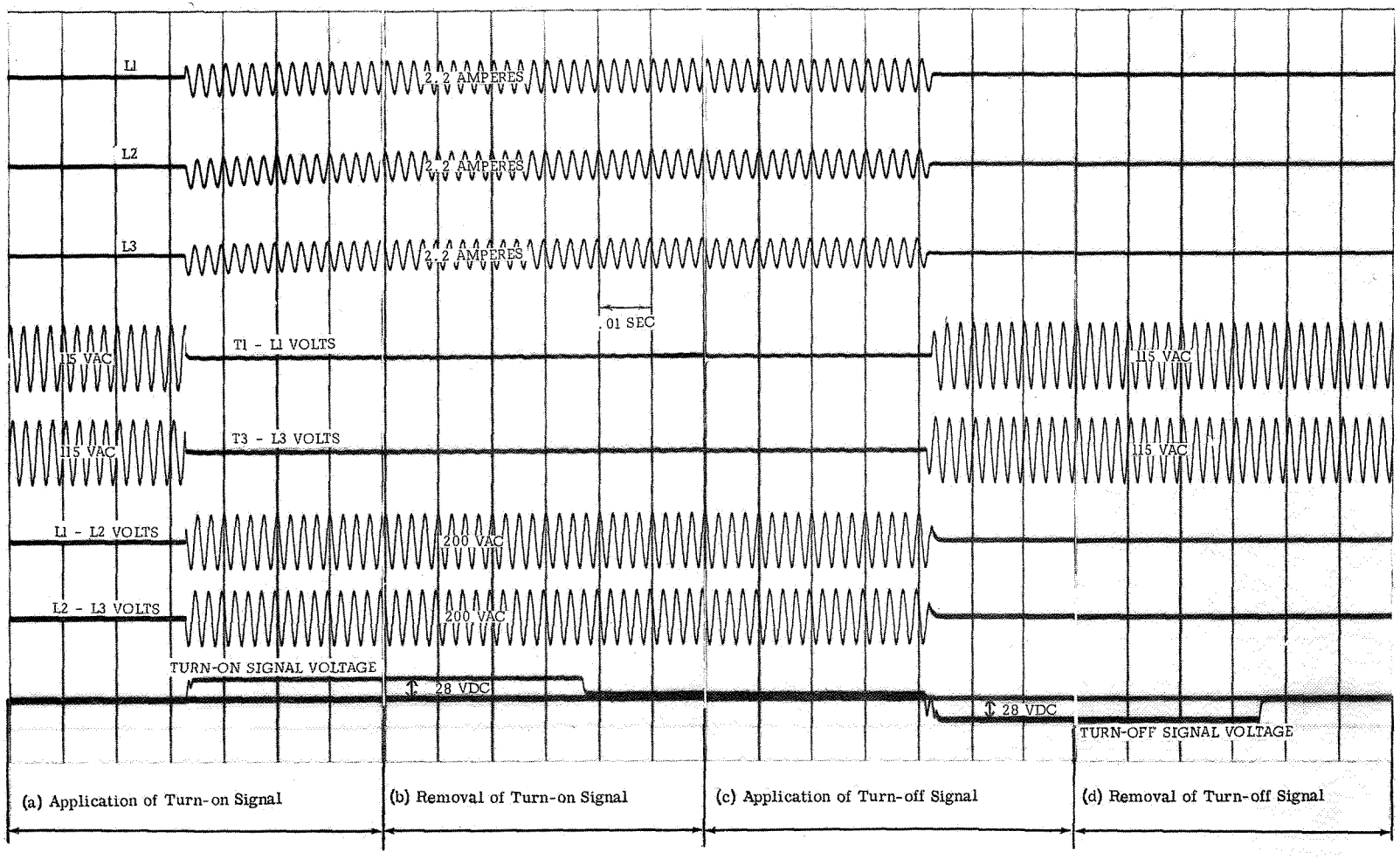
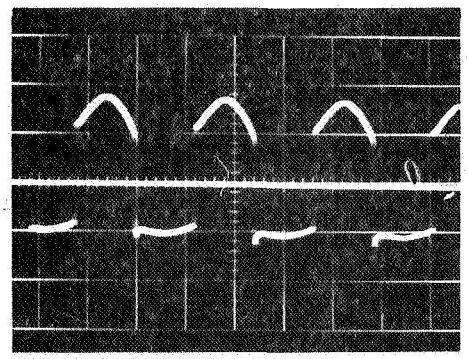
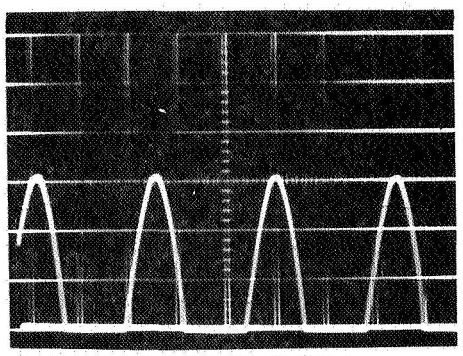


Figure 33. - Inverter System Static Contactor Oscillogram of Inductive-Resistive Load, Line Current 0 to 2.2 to 0 Amperes

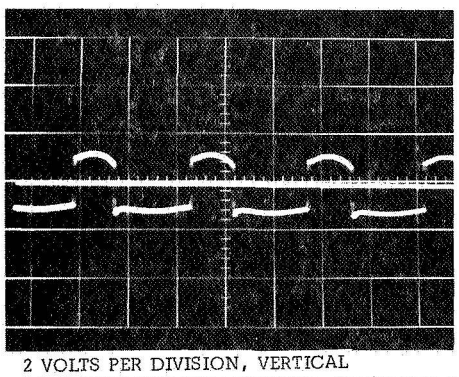


1 VOLT PER DIVISION, VERTICAL
1 MILLISECOND PER DIVISION, HORIZONTAL

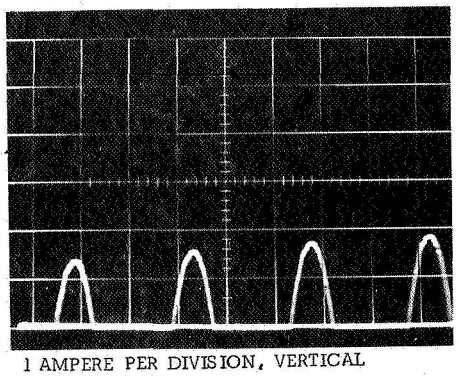


1 AMPERE PER DIVISION, VERTICAL
1 MILLISECOND PER DIVISION, HORIZONTAL

0 to 2.2 AMPERES, RESISTIVE LOAD

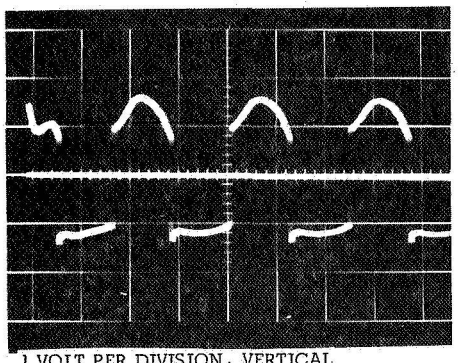


2 VOLTS PER DIVISION, VERTICAL
1 MILLISECOND PER DIVISION, HORIZONTAL

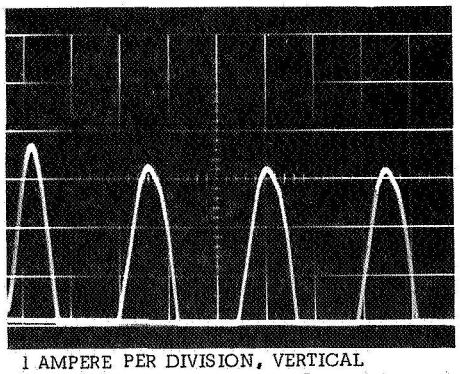


1 AMPERE PER DIVISION, VERTICAL
1 MILLISECOND PER DIVISION, HORIZONTAL

0 to 2.2 AMPERES, .75 LAGGING POWER FACTOR



1 VOLT PER DIVISION, VERTICAL
1 MILLISECOND PER DIVISION, HORIZONTAL



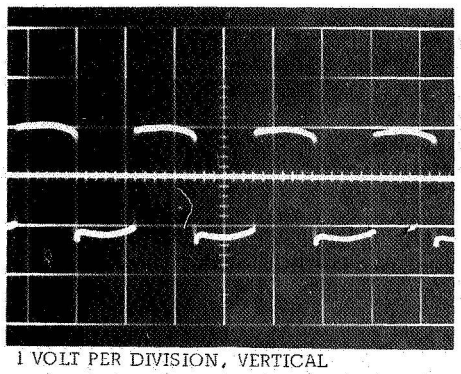
1 AMPERE PER DIVISION, VERTICAL
1 MILLISECOND PER DIVISION, HORIZONTAL

0 to 2.2 AMPERES, .75 LEADING POWER FACTOR

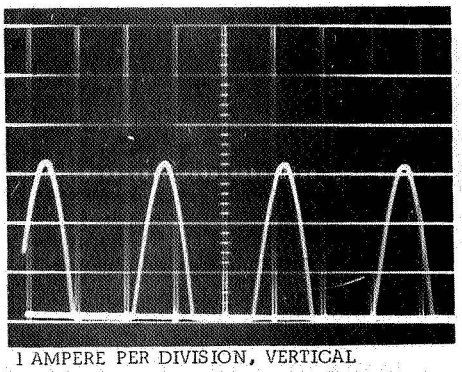
VOLTAGE TRANSIENTS
SCR#1

CURRENT TRANSIENTS
SCR#1

Figure 34. - Inverter System Static Contactor. Voltage and Current Transients of Power Contact, SCR #1, During Load Application

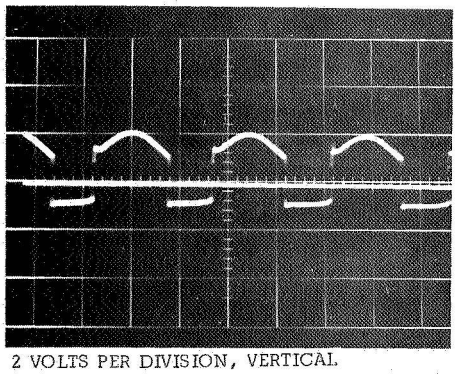


1 VOLT PER DIVISION, VERTICAL
1 MILLISECOND PER DIVISION, HORIZONTAL

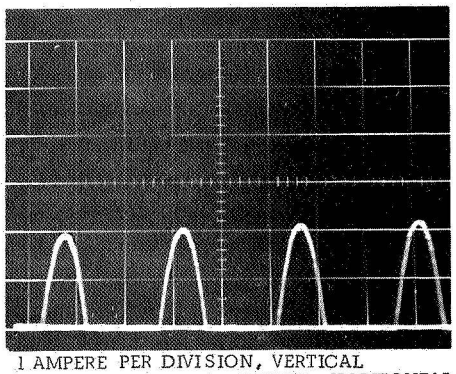


1 AMPERE PER DIVISION, VERTICAL
1 MILLISECOND PER DIVISION, HORIZONTAL

0 to 2.2 AMPERES, RESISTIVE LOAD

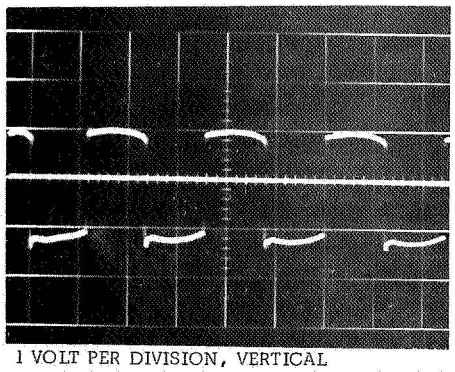


2 VOLTS PER DIVISION, VERTICAL
1 MILLISECOND PER DIVISION, HORIZONTAL

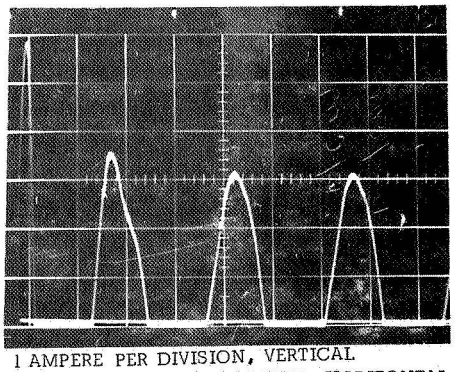


1 AMPERE PER DIVISION, VERTICAL
1 MILLISECOND PER DIVISION, HORIZONTAL

0 to 2.2 AMPERES, .75 LAGGING POWER FACTOR



1 VOLT PER DIVISION, VERTICAL
1 MILLISECOND PER DIVISION, HORIZONTAL



1 AMPERE PER DIVISION, VERTICAL
1 MILLISECOND PER DIVISION, HORIZONTAL

0 to 2.2 AMPERES, .75 LEADING POWER FACTOR

VOLTAGE TRANSIENTS
SCR# 2

CURRENT TRANSIENTS
SCR# 2

Figure 35. - Inverter System Static Contactor. Voltage and Current Transients of Power Contact, SCR #2, During Load Increase

2.2 ampere, rms, balanced resistive load. The load current was then increased to 2.75 amperes per phase and maintained at this value for five minutes. Contactor currents, wattages, and input and output voltages were recorded after controlled rectifier temperature stabilization and at the beginning and end of the five-minute interval. The controlled rectifier case temperatures increased by approximately 3°F above the stabilized temperatures of 91° to 95°F during the five-minute, 125-percent-load application. to The recorded voltage drops across the power contacts remained essentially unchanged for the load currents of 2.2 and 2.75 amperes. With the conduction and interruption of 2.75 amperes per phase performed without exceeding the temperature ratings of SCR1, SCR3, and SCR5, contactor operation for a 125-percent load is concluded to be satisfactory.

Overload application and removal: After the cases of SCR1, SCR3, and SCR5 were temperature stabilized at a three-phase, balanced line current of 2.2 amperes, rms, resistive, capacitive-resistive, and inductive-resistive load oscillograms were taken of current increase to 4.4 amperes and load removal. Figures 36, 37, and 38 are the oscillograms of load current increase from 2.2 to 4.4 amperes and load removal from 4.4 to zero for the resistive, capacitive-resistive, and inductive-resistive loads, respectively. The static contactor interrupted the 4.4 ampere load one minute after application. After one minute at 4.4 amperes, the case temperatures of SCR1, SCR3, and SCR5 measured 96 to 102°F.

Figures 39 and 40 show oscilloscope pictures of the current through and the voltage across the power contact SCR1 and SCR2 with resistive, inductive-resistive, and capacitive-resistive load current increase from 2.2 to 4.4 amperes, rms after the case temperature of SCR1 was stabilized at 2.2 amperes. As stated previously, the unsymmetrical voltage drop across the controlled rectifiers is a result of the current probe in series with the cathode of the controlled rectifier. Also, because the current and voltage photographs were not taken simultaneously, direct comparisons cannot be made.

Figures 41, 42 and 43 are the oscillograms of load current increase from 2.2 to 5.5 amperes, rms and load removal from 5.5 amperes to zero for the resistive, capacitive-resistive, and inductive-resistive loads, respectively. The static contactor interrupted the 5.5-ampere short-circuit current 800 milliseconds after application with a mechanical contactor operating 200 milliseconds later.

The oscilloscope pictures of transient current through and the voltage drop across the power contact SCR1 and SCR2 with resistive, inductive-resistive, and capacitive-resistive load current increase from 2.2 to 5.5 amperes, rms, after the case of SCR1 was

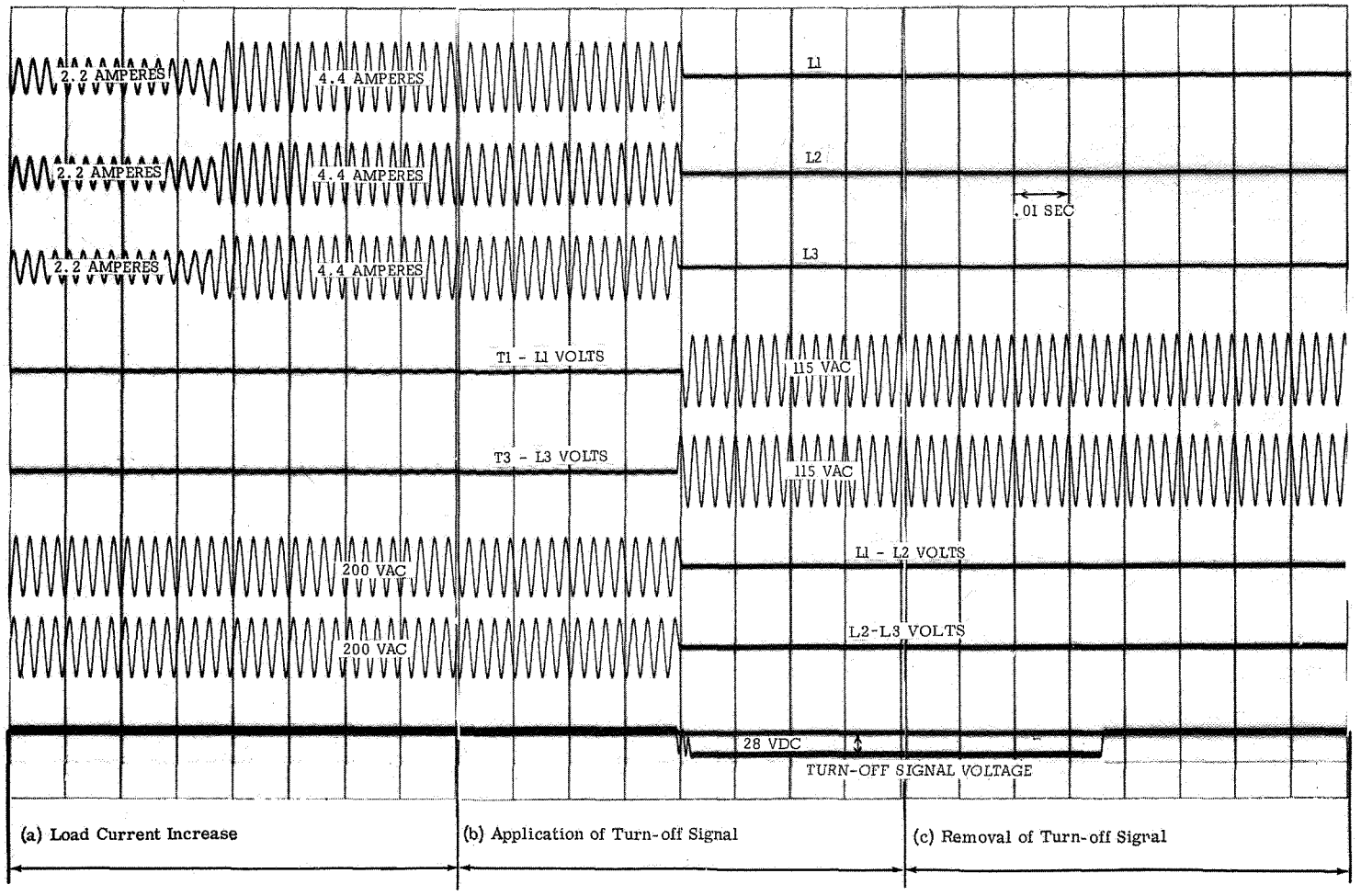


Figure 36. - Inverter System Static Contactor Oscillogram of Resistive Load, Line Current 2.2 to 4.4 to 0 Amperes

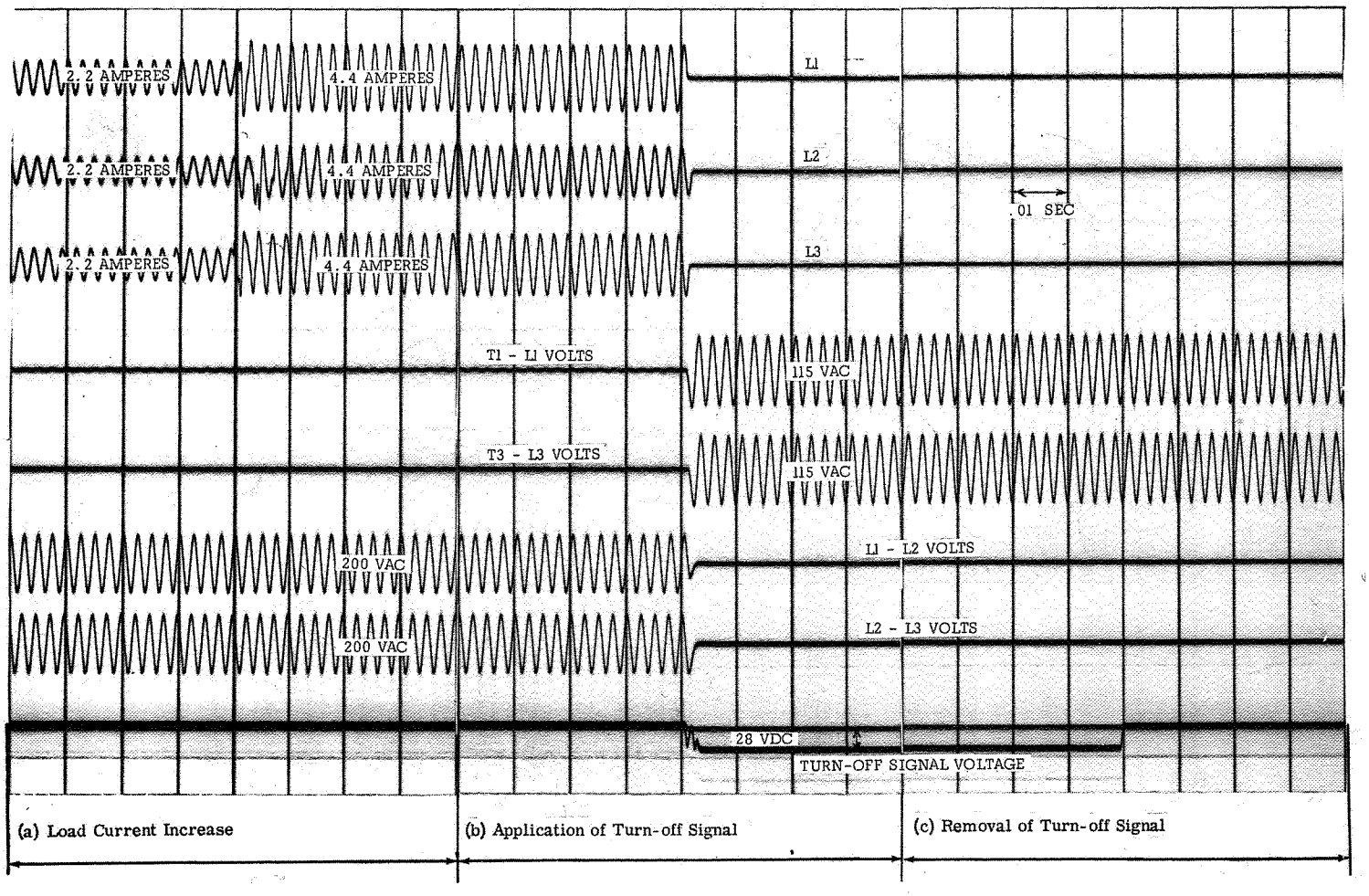


Figure 37. - Inverter System Static Contactor Oscillogram of Capacitive-Resistive Load, Line Current 2.2 to 4.4 to 0 Amperes

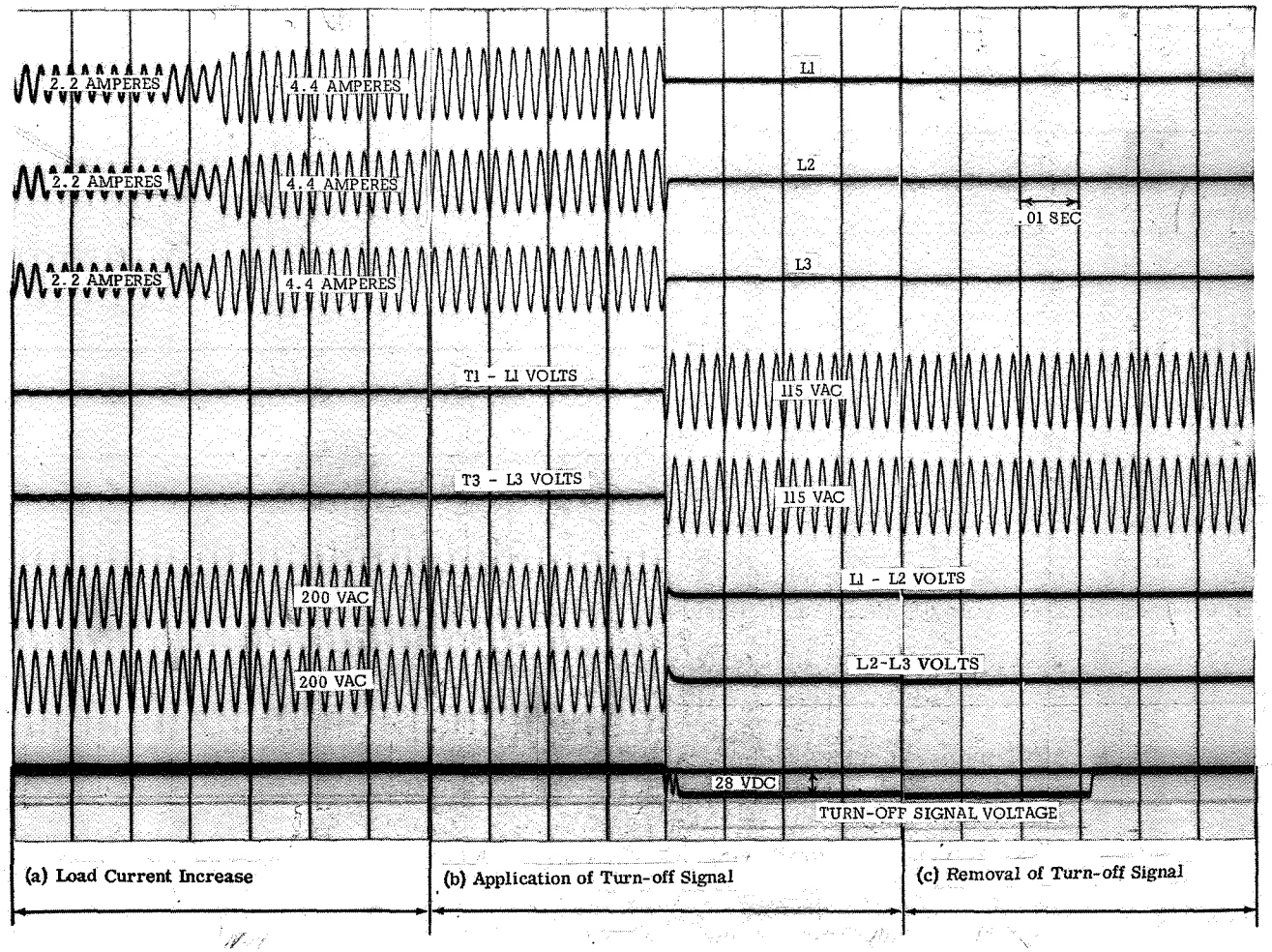
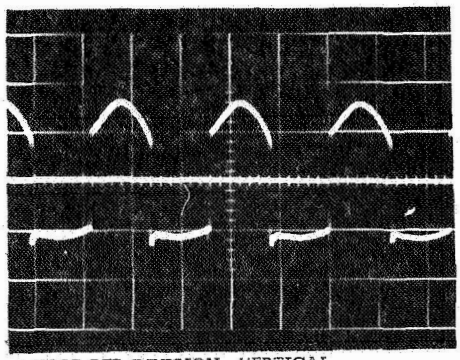
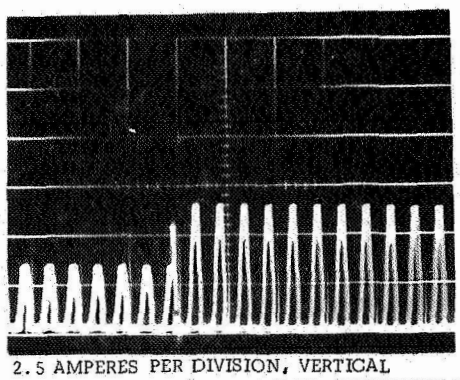


Figure 38. - Inverter System Static Contactor Oscillogram of Inductive-Resistive Load, Line Current 2.2 to 4.4 to 0 Amperes

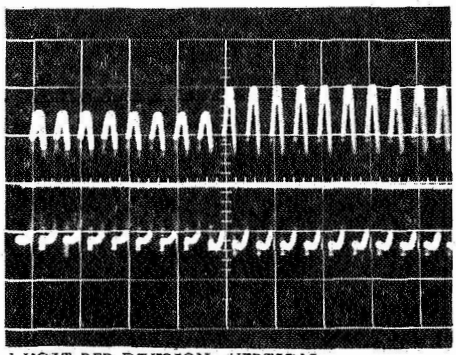


1 VOLT PER DIVISION, VERTICAL
1 MILLISECOND PER DIVISION, HORIZONTAL

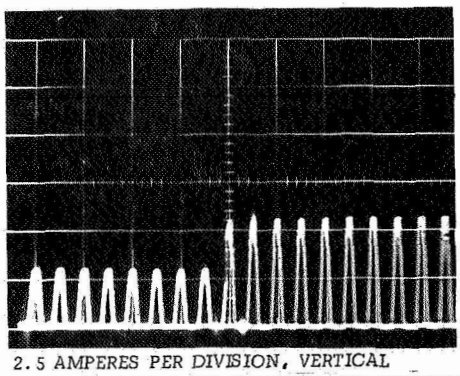


2.5 AMPERES PER DIVISION, VERTICAL
5 MILLISECONDS PER DIVISION, HORIZONTAL

2.2 to 4.4 AMPERES, RESISTIVE LOAD

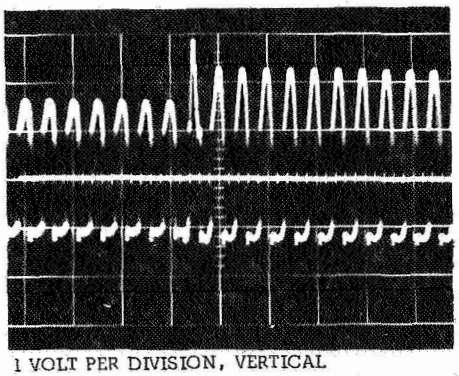


1 VOLT PER DIVISION, VERTICAL
5 MILLISECONDS PER DIVISION, HORIZONTAL

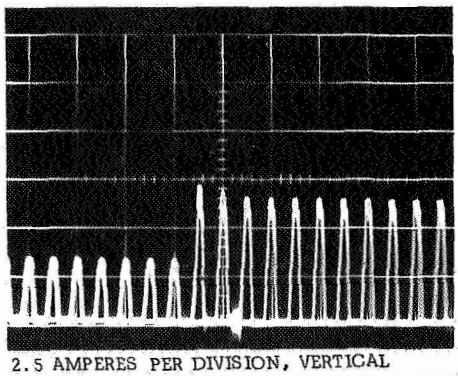


2.5 AMPERES PER DIVISION, VERTICAL
5 MILLISECONDS PER DIVISION, HORIZONTAL

2.2 to 4.4 AMPERES, .75 LAGGING POWER FACTOR



1 VOLT PER DIVISION, VERTICAL
5 MILLISECONDS PER DIVISION, HORIZONTAL



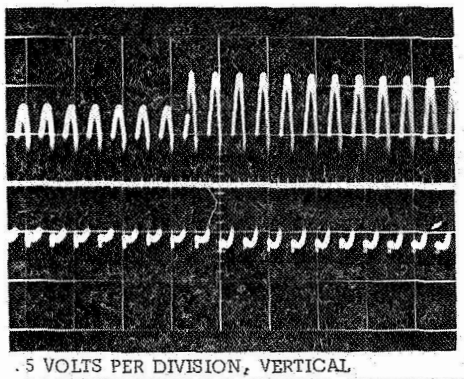
2.5 AMPERES PER DIVISION, VERTICAL
5 MILLISECONDS PER DIVISION, HORIZONTAL

2.2 to 4.4 AMPERES, .75 LEADING POWER FACTOR

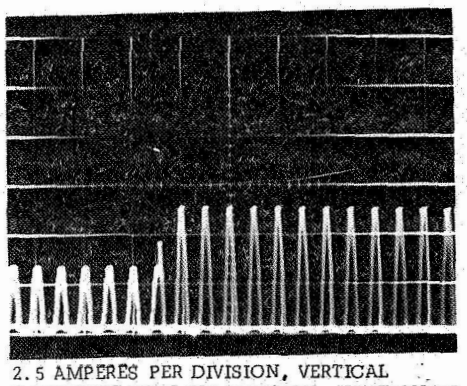
VOLTAGE TRANSIENTS
SCR#1

CURRENT TRANSIENTS
SCR#1

Figure 39. - Inverter System Static Contactor. Voltage and Current Transients of Power Contact, SCR #1, During Load Increase

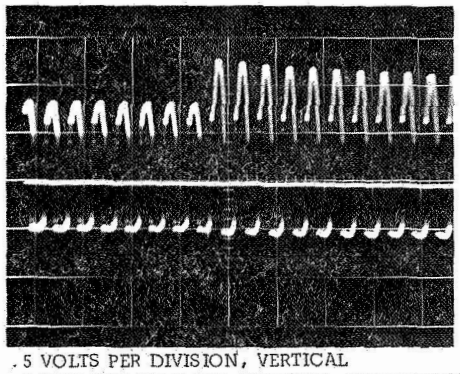


.5 VOLTS PER DIVISION, VERTICAL
5 MILLISECONDS PER DIVISION, HORIZONTAL

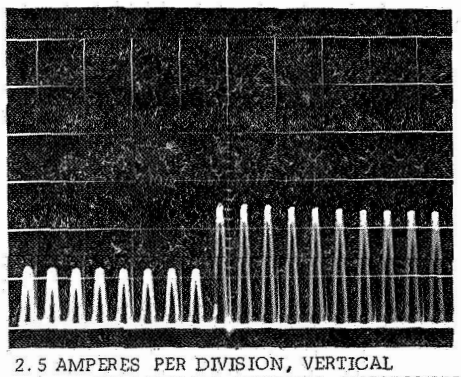


2.5 AMPERES PER DIVISION, VERTICAL
5 MILLISECONDS PER DIVISION, HORIZONTAL

2.2 to 4.4 AMPERES, RESISTIVE LOAD

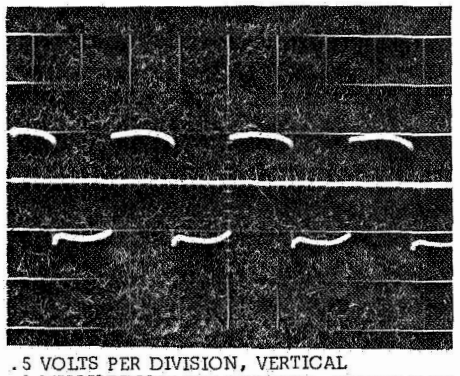


.5 VOLTS PER DIVISION, VERTICAL
5 MILLISECONDS PER DIVISION, HORIZONTAL

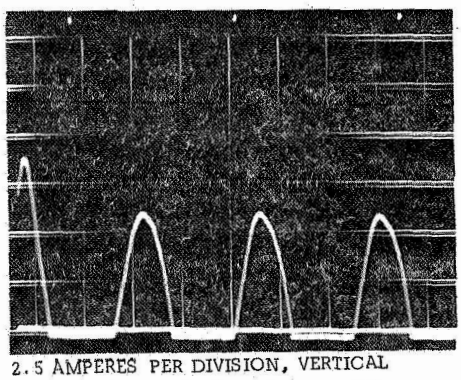


2.5 AMPERES PER DIVISION, VERTICAL
5 MILLISECONDS PER DIVISION, HORIZONTAL

2.2 to 4.4 AMPERES, .75 LAGGING POWER FACTOR



.5 VOLTS PER DIVISION, VERTICAL
1 MILLISECOND PER DIVISION, HORIZONTAL



2.5 AMPERES PER DIVISION, VERTICAL
1 MILLISECOND PER DIVISION, HORIZONTAL

2.2 to 4.4 AMPERES, .75 LEADING POWER FACTOR

VOLTAGE TRANSIENTS
SCR# 2

CURRENT TRANSIENTS
SCR# 2

Figure 40. - Inverter System Static Contactor. Voltage and Current Transients of Power Contact, SCR #2, During Load Increase

temperature stabilized at the 2.2 ampere load, are shown in figures 44 and 45. The remarks regarding the unsymmetrical voltage drop across the controlled rectifiers, because of the current probe in series with the controlled rectifiers, are applicable here. Also, direct comparisons of the displayed voltage and current cannot be made because the photographs were not taken simultaneously.

Contactor maximum continuous current rating: The controlled rectifier and heat sink combination used for the inverter system contactors makes it possible for the contactor to conduct greater currents than required for this application. The controlled rectifier used is a standard unit which provides a greater current capability without a weight or size penalty. It was the purpose of this test to determine the maximum current rating the static contactor could conduct continuously without exceeding the junction temperature rating of the controlled rectifier contacts. The results of this test can be used, with some established safety factor, depending on the application, to obtain the current rating of the contactor. It should be recognized that the results obtained are for a given controlled rectifier heat sink and breadboard configuration.

The test was performed with the static contactor connected to an adjustable, balanced, three-phase resistive load. With the line-to-line voltages across the contactor output terminals at 200 volts rms, the contactor was subjected to the rms line currents given in table III. Corresponding maximum case temperatures are listed which permit the controlled rectifiers to operate at the maximum rated junction temperature of 257°F (125°C). With the listed load current conducted by the contactor, the cases of SCR1, SCR3, and SCR5 were temperature stabilized without exceeding the tabulated maximum value. The laboratory measured case temperatures, including room ambient temperature, are presented in table III for the corresponding load currents. Contactor voltages, currents, and temperatures were recorded before and after temperature stabilization of the controlled rectifiers. It was established that the contactor could "open" and "close" on each load current before proceeding to the next load value.

Cycling test: With a three-phase, balanced, resistive load adjusted to 2.2 amperes, rms and the voltage across the contactor output terminals at 200 volts line-to-line, the cases of SCR1, SCR3, and SCR5 were temperature stabilized. Contactor voltages, currents and wattages were recorded before and after temperature stabilization of the controlled rectifiers. After temperature stabilization, the contactor was cycled on and off for a total of 50 cycles such that the contactor was on for 10 seconds and off for 0.25 seconds. The cycling test was considered successful because the static switch applied and removed load from the power source without failure.

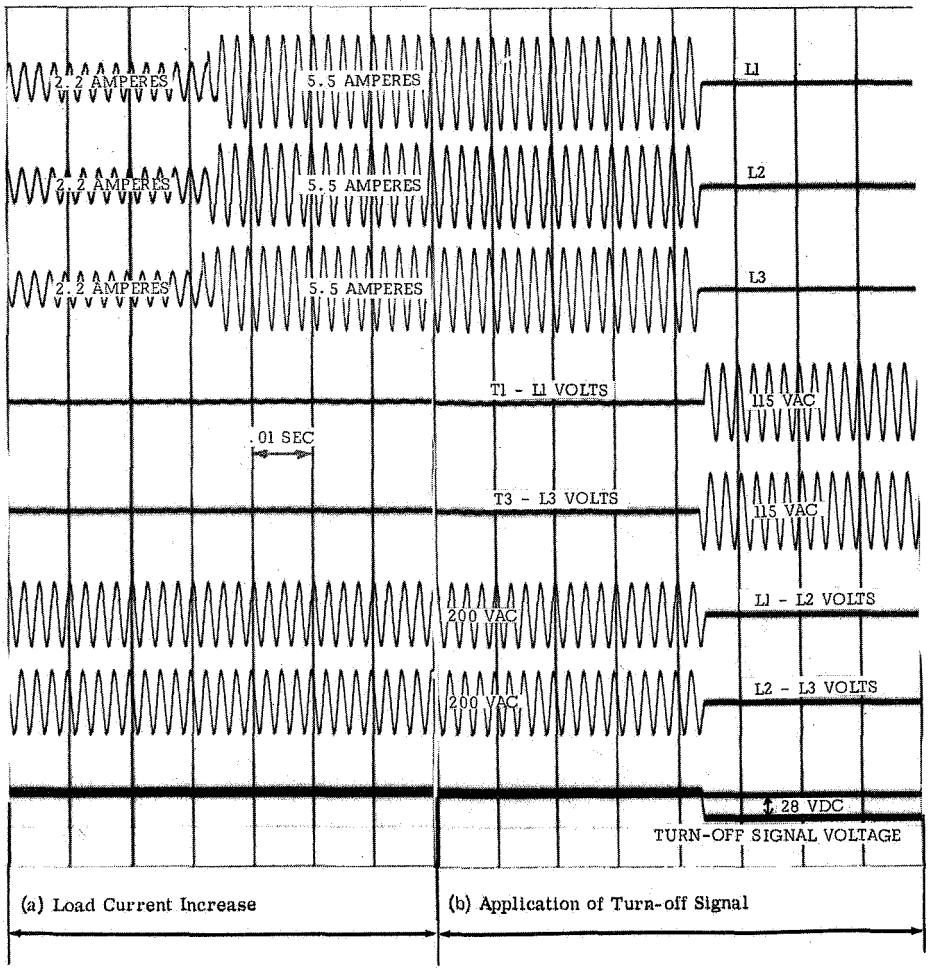


Figure 41. - Inverter System Static Contactor Oscillogram of Resistive Load, Line Current 2.2 to 5.5 to 0 Amperes

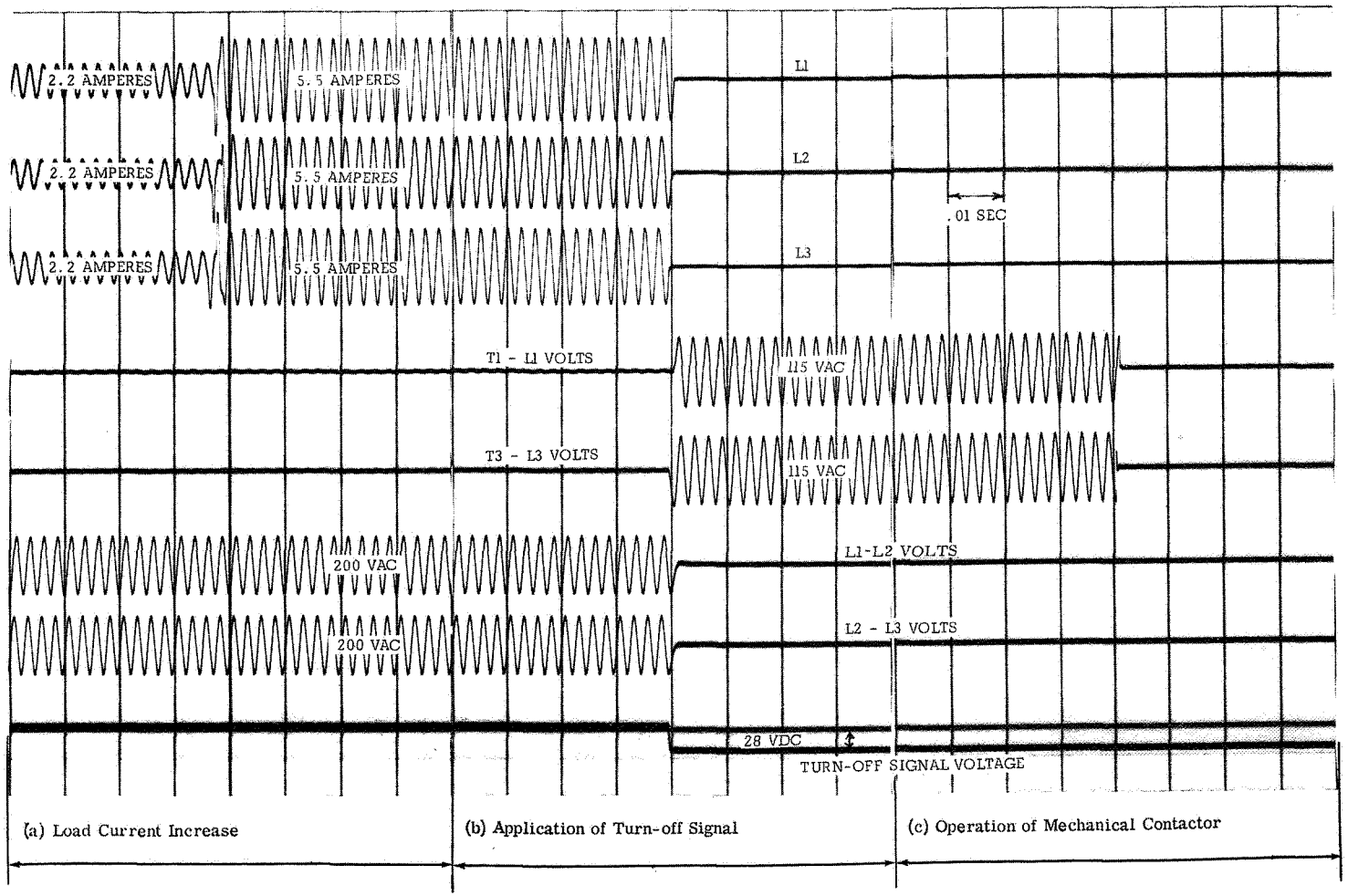


Figure 42. - Inverter System Static Contactor Oscillogram of Capacitive-Resistive Load, Line Current 2.2 to 5.5 to 0 Amperes

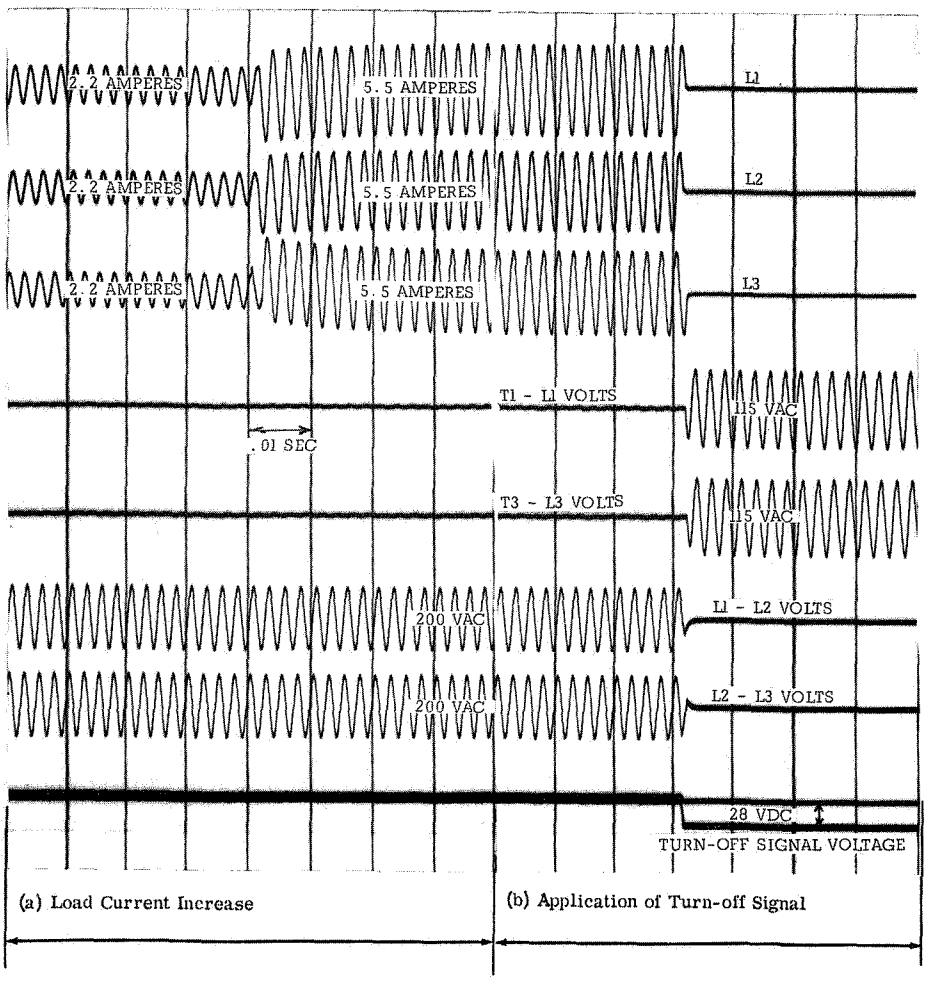
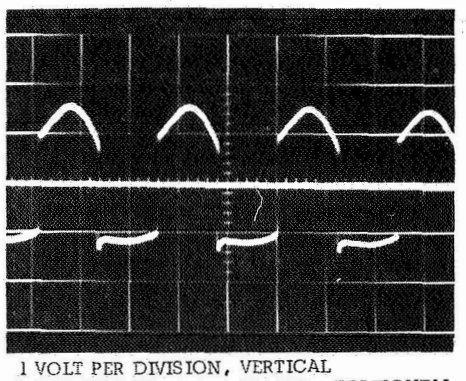
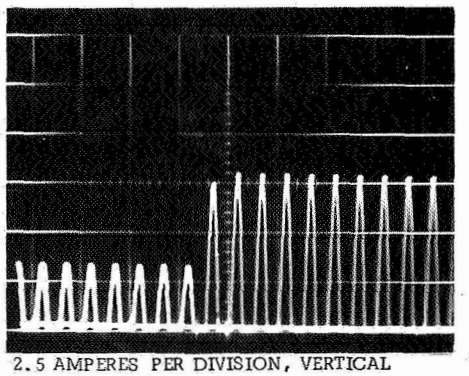


Figure 43. - Inverter System Static Contactor Oscillogram of Inductive-Resistive Load, Line Current 2.2 to 5.5 to 0 Amperes

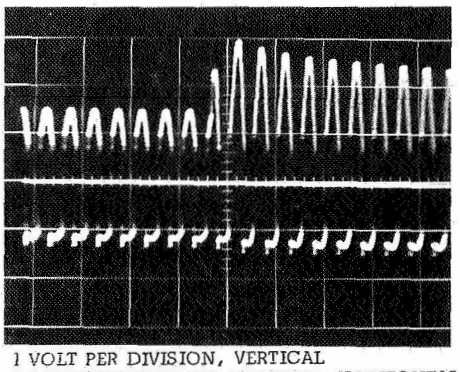


1 VOLT PER DIVISION, VERTICAL
1 MILLISECOND PER DIVISION, HORIZONTAL

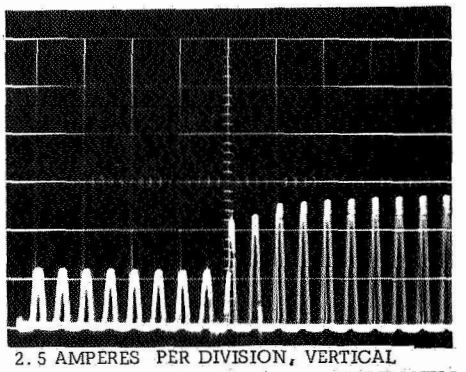


2.5 AMPERES PER DIVISION, VERTICAL
5 MILLISECONDS PER DIVISION, HORIZONTAL

2.2 to 5.5 AMPERES, RESISTIVE LOAD

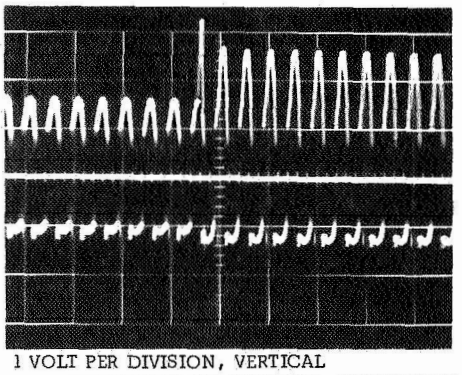


1 VOLT PER DIVISION, VERTICAL
5 MILLISECONDS PER DIVISION, HORIZONTAL

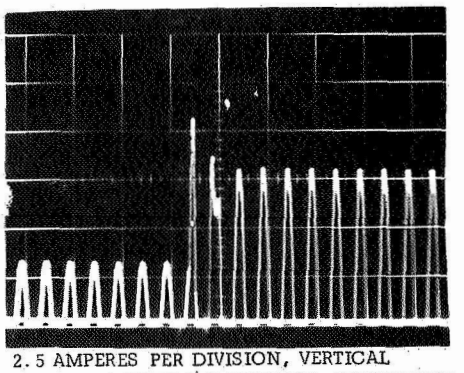


2.5 AMPERES PER DIVISION, VERTICAL
5 MILLISECONDS PER DIVISION, HORIZONTAL

2.2 to 5.5 AMPERES, .75 LAGGING POWER FACTOR



1 VOLT PER DIVISION, VERTICAL
5 MILLISECONDS PER DIVISION, HORIZONTAL



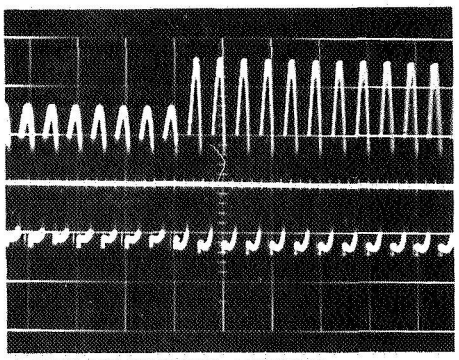
2.5 AMPERES PER DIVISION, VERTICAL
5 MILLISECONDS PER DIVISION, HORIZONTAL

2.2 to 5.5 AMPERES, .75 LEADING POWER FACTOR

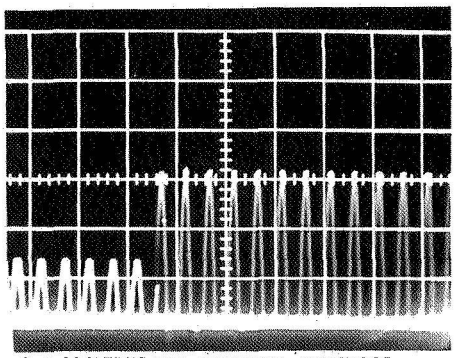
VOLTAGE TRANSIENTS
SCR# 1

CURRENT TRANSIENTS
SCR# 1

Figure 44. - Inverter System Static Contactor. Voltage and Current Transients of Power Contact, SCR #1, During Load Increase

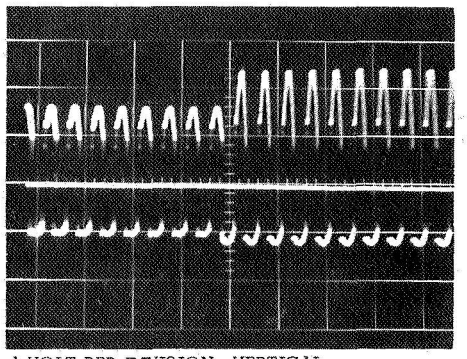


1 VOLT PER DIVISION, VERTICAL
5 MILLISECONDS PER DIVISION, HORIZONTAL

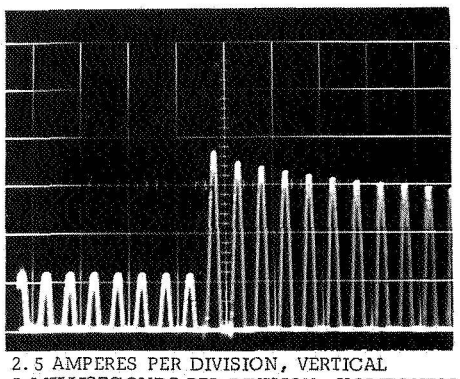


2.5 AMPERES PER DIVISION, VERTICAL
5 MILLISECONDS PER DIVISION, HORIZONTAL

2.2 to 5.5 AMPERES, RESISTIVE LOAD

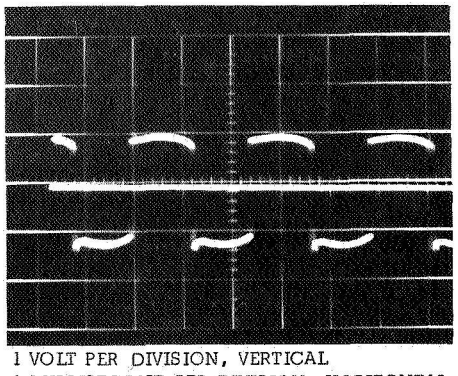


1 VOLT PER DIVISION, VERTICAL
5 MILLISECONDS PER DIVISION, HORIZONTAL

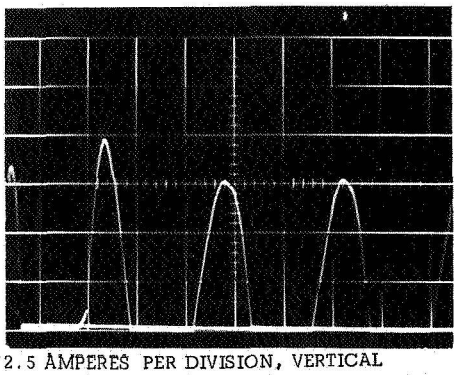


2.5 AMPERES PER DIVISION, VERTICAL
5 MILLISECONDS PER DIVISION, HORIZONTAL

2.2 to 5.5 AMPERES, .75 LAGGING POWER FACTOR



1 VOLT PER DIVISION, VERTICAL
1 MILLISECOND PER DIVISION, HORIZONTAL



2.5 AMPERES PER DIVISION, VERTICAL
1 MILLISECOND PER DIVISION, HORIZONTAL

2.2 to 5.5 AMPERES, .75 LEADING POWER FACTOR

VOLTAGE TRANSIENTS
SCR# 2

CURRENT TRANSIENTS
SCR# 2

Figure 45. - Inverter System Static Contactor. Voltage and Current Transients of Power Contact, SCR #2, During Load Increase

Table III. - Inverter System LBC, LCC, and TBC Maximum Current Rating as Function of Power Contact Temperature

Line Current (amps, rms)	Maximum SCR Case Temperature (°F)	Measured Case Temperature SCR5 [a] (°F)	Case Temperature Rise SCR5 (°F)
5.5	228	114	35
6.7	223	123	43
8.9	210	133	54
11.1	196	147	69
13.3	181	159	78
15.5	165	165 [b]	35

(a) The case temperature of SCR5 was the highest of the three monitored.

(b) The maximum allowable case temperature was reached 3 minutes after the load was applied.

Reliability

Reliability of static contactors. - Reliability analyses have been made on the dc and ac static contactor engineering verification models presented in this report. The reliability analyses were based on the assumption that the exponential distribution $R = e^{-t/m}$ is the applicable mathematical model where R is the reliability (probability of failure-free operation), m is the mean time between failures (MTBF), t is the time being considered, and e is the base of natural logarithm. Past experience on static electric equipment justifies the assumption of the exponential distribution (ref. 6).

The MTBF calculations were made considering all parts in the breadboard design with a 100 percent duty cycle, stressed 100 percent of the time. The ICC/CCC for these conditions has a failure rate of 0.88002 percent failures per 1000 hours, which is an equivalent MTBF of 113,634 hours. This compares to the inverter system LBC, LCC, and TBC mean time between failure of 68,899 hours and a failure rate of 1.45138 percent failures per 1000 hours.

The calculated MTBF can be improved by, first, considering a duty cycle of less than 100 percent for those parts used in the control circuit and, second, by using high-reliability components throughout the circuit.

Considering first the use of commercial-grade components with a one percent duty cycle for the control circuit, the failure rate of the ICC/CCC is 0.380702 percent failures per 1000 hours with an MTBF of 262,672 hours. For the same conditions, the inverter system LBC, LCC and TBC failure rate is 1.2654 failures per 1000 hours with an MTBF of 79,026 hours.

With high-reliability parts and with a 100 percent duty cycle, the failure rate of the ICC/CCC becomes 0.79338 percent failures per 1000 hours with an associated MTBF of 126,652 hours. The corresponding failure rate for the inverter system LBC, LCC and TBC is 0.72262 percent failures per 1000 hours with a MTBF of 138,385 hours.

With high-reliability parts and a one percent duty cycle for the control circuit, the failure rate of the ICC/CCC becomes 0.32381 percent failures per 1000 hours with an associated MTBF of 311,711 hours. The failure rate of the inverter system LBC, LCC and TBC is 0.66885 percent failures per 1000 hours with a MTBF of 149,510 hours.

Reliability of mechanical contactors. - Military Specification MS 24140 provides the requirements for a mechanical contactor which most closely matches the electrical rating of the static, direct current ICC/CCC. One contactor which meets this specification is a single-pole, single-throw, electrically held, hermetically sealed unit. The quoted reliability data for this contactor is a mean cycles between failures (MCBF) of 140,000 hours at a confidence level of 90 percent. The calculated mean time between failures (MTBF) for the given MCBF is 116,713 hours.

Military Specification MS 25467 established the requirements for a mechanical relay which compares to the electrical rating of the static, alternating current inverter system LBC, LCC, and TBC. One relay which meets this specification is a four-pole, double-throw, magnetically latched, hermetically sealed unit. Based on the reported failure rate of 0.346 percent failures per 10,000 cycles, at a confidence level of 90 percent, the calculated MTBF is 2410 hours and the MCBF is 28,902 cycles (ref. 7). These values were calculated using the standard cycling rate of 20 cycles per minute as established in MIL-R-6016, General Specification for Aerospace Electric Relays.

Comparison of Static and Mechanical Contactors

Some of the electrical and physical characteristics of the breadboarded static engineering verification models of this program are compared with comparably rated production designed mechanical contactors in tables IV and V. Although a comparison can be obtained from the tables with respect to the electrical performance

Table IV. - Comparison of Static and Mechanical DC Contactors

	Mechanical Contactor	Static Contactor
Contact		
System Voltage, Nominal (volts)	28	28
Design Current Rating (amps)	50	40
Current Overload (amps)	100, 1 minute	100, 1 second
Contact Voltage Drop (volts)	0.05 to 0.1	1 to 1.5
Duration of Contact Bounce, Max. (milliseconds)	2	0
Contact Latching	electrically held	self-latching
Control Circuit	28	28
Voltage, Nominal (volts)	8.6	0
Power, Continuous (watts)	10	0.8
Release Time, Max. (milliseconds)		
Weight (lbs.)		
Packaged	0.9	--
Components Only	--	2.7
Dimensions (inches)	2.84x2.7x2.67	--
Reliability, MTBF (hours)	116,713	311,711[a]

(a) One percent duty cycle considered for control circuit parts with high-reliability components used for approximately 50 percent of design.

of the two contactor types, it is obvious that only an estimate of the true comparison of the physical properties, such as weights and sizes can be achieved. From the tables it is seen that the static contactor's greatest advantage, particularly for space electrical power systems, is its potentially greater mean time between failures with its corresponding greater value of mean cycles between failures. Other advantages of the static contactor which may be equally important are faster response and no contact bounce, which would be particularly desirable in severe environments of mechanical shock and vibration.

As shown in tables IV and V the principal disadvantages of the static contactors, compared with their electromagnetic counterparts, are the higher contact voltage drops and the obviously greater packaged weights and volumes which will result, even with refinement. Another possible disadvantage of static contactors, not specifically shown in the tables, is their lack of complete electric power circuit isolation, in the "open" condition, between

Table V. - Comparison of Static and Mechanical AC Contactors

	Mechanical Contactor	Static Contactor
Contacts		
System Voltage, Single Phase, Nominal (volts)	115	115
Design Current Rating (amps)	5	2.2
Current Overload (amps)	1 minute	3 minutes
Duration of Contact Bounce, Max. (milliseconds)	2	0
Contact Latching	magnetically held	electrically held
Control Circuit		
Voltage, Nominal (volts, dc)	28	28
Power, Continuous (watts)	0	23.7
Operating Time, Max. (milliseconds)	20	less than 1
Weight (lbs.)		
Packaged	0.35	--
Components Only	--	1.04
Dimensions (inches)	1.531x1.031x.175	--
Reliability, MTBF (hours)	2,410	149,510[a]

(a) One percent duty cycle considered for control circuit parts with high-reliability components used for approximately 50 percent of design.

the line and load as achieved by mechanical contactors. A leakage current from a few microamperes to several milliamperes may flow depending on the characteristics and rating of the selected switching device for the power contact.

Although static contactors compared with mechanical contactors (particularly special designs) are more susceptible to nuclear radiation and are limited to an operating temperature less than 125°C (junction temperature capacity of controlled rectifiers), these limitations have been circumvented for other semiconductor equipment in earlier space electric power systems studies.

Static Switches Concluding Remarks

The electrical characteristics and the feasibility of controlling ac and dc electric power with static switches have been

verified. Electrical testing of a three-phase, ac switch rated at 2.2 amperes and 115 volts per phase demonstrated that such a switch will handle 250 percent of its rated current for power factor loads ranging from 0.75 lagging to 0.75 leading. Interruption times for currents up to 250 percent of rated are approximately one millisecond.

Electrical testing of a dc switch rated at 40 amperes and 28 volts demonstrated that such a switch will handle 250 percent of its rated load current. Interruption of rated load current is achieved in approximately one millisecond; overload currents are interrupted in approximately 2 to 3 milliseconds.

Static switch advantages, such as faster response, repeated cycling, no arcing, and long life, have been discussed in comparison with its electromagnetic counterpart.

It has been shown that a static switch, when compared with its mechanical counterpart, would weigh more, have a greater volume, and dissipate more power because of its greater contact voltage drop. The static switch will be more reliable than the mechanical contactor because of its longer mean-time-between failures (MTBF) which, calculations show, can be increased further by the use of high-reliability components.

ANNUNCIATOR

Annunciator Functions

The purpose of an annunciator is to provide a system operator with information concerning the state of an electric power system. For example, the basic system configuration shown in figure 1 can be operated as a parallel system or as separate isolated systems. An additional function of the annunciator is to inform the system operator as to the location and type of faults occurring in the system. Such information is used by the operator to determine suitable action for maintaining peak system operation.

The annunciator consists of lamps which are energized by either static switches or by auxiliary contacts of the power contactor. The annunciator provides information to the system operator as to the state of each mechanical contactor, whether the system is in an isolated or paralleled mode, and, should a fault occur, what type of fault. Since this study involved both ac (inverter) and dc (converter) systems, the annunciator also indicated which type of system the annunciator was connected to. See reference 2 for a description of the control and protection circuits. The annunciator panel was made compatible with either ac or dc systems. The annunciator provides indication for only one

channel or subsystem. Hence, an annunciator panel is provided for each subsystem. Figure 46 shows a block diagram of the annunciator functions relative to the remainder of the subsystem.

The type of subsystem (inverter or converter) connected to the annunciator is determined by the wiring arrangement of a connector. The appropriate lamp is lit by simply grounding the lamp through the connector.

Subsystem operating mode is shown by lamps connected to contacts of a manual switch used to select the manual or automatic mode of system operation. This switch is included as part of the annunciator.

The state of the system is indicated in two ways. First a lamp associated with each contactor is lit when the contactor is closed. The lamp is lit by auxiliary contacts of the contactor. A second indication is provided by lamps indicating whether the system is paralleled or isolated. The paralleled state is achieved only when all three of the contactors, shown in figure 1, of a subsystem are closed. The paralleled state means that the subsystem is capable of supplying power to its associated load and to aid in supplying power to other subsystem load busses as required. The isolated state is indicated only when the tie-bus contactor of figure 1 is tripped while the rest of the subsystem contactors are closed. The isolated state means that the subsystem can supply power only to its load bus.

Abnormal or fault conditions are determined by the subsystem control and protection circuit. A lamp representing each protective function is provided. There are six lamps required for the dc subsystem while the ac system requires three additional lamps for the frequency protection circuits.

One or more signals from the protective circuits are required by the annunciator lamp-drive to operate the proper lamps. A combination of signals prevents a lamp from flickering during a transient fault condition and prevents multiple lamps from being lighted when a subsystem is shut down, either intentionally or by a fault condition. The faults normally encountered when a subsystem is shutdown are an undervoltage and, for the inverter subsystem, underfrequency. The following sections will describe the circuits used to operate the fault lamps and the logic signals from the control and protection circuits necessary to light a particular fault lamp.

Selection of Lamp-Drive Circuit

Three approaches were analyzed as means for achieving visual indication of subsystem fault conditions. All three methods use

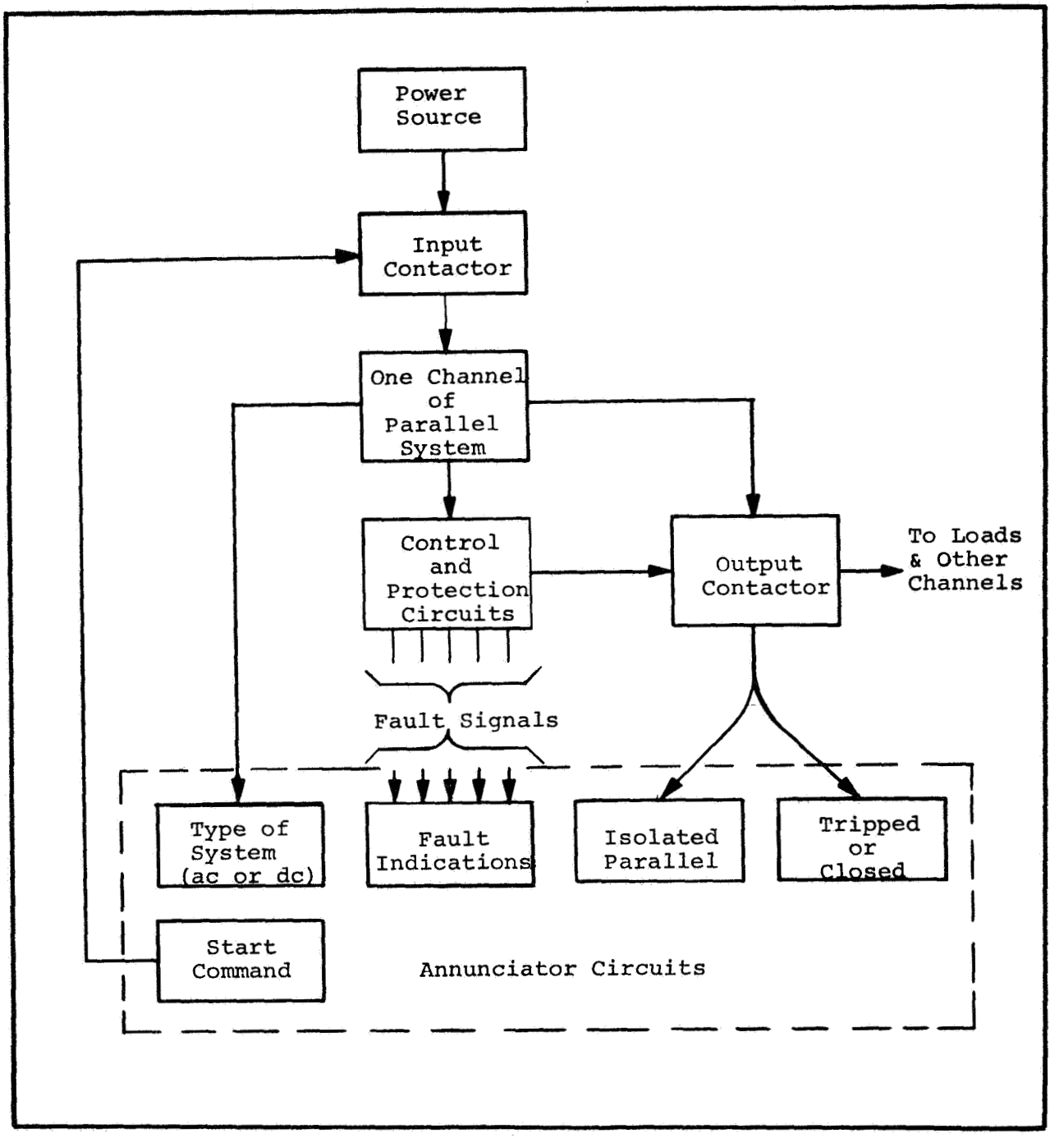


Figure 46. - Signal Sources for Annunciator Functions

AND logic to determine when to light a particular fault lamp, but the required amplification is achieved in different ways. Of the three approaches, the silicon controlled rectifier (SCR) lamp-drive is the simplest and most efficient and imposes less loading on the control and protection circuits. Table VI summarizes the results of this comparison and clearly shows the SCR lamp-drive to be superior.

SCR lamp-drive circuit. - Figure 47 shows the basic schematic of a visual annunciator using SCR's as the lamp-control device. The resistor and diode configuration connected to the SCR gate provide logic control (AND gate) and gate drive for the SCR. The two diodes connected between the cathodes of the SCR's and ground provide a reverse bias on the SCR when one or more of the gate diodes are grounded. The reverse bias prevents false triggering of an SCR. Another attractive feature of the SCR, in this application, is its latching effect: a lamp will remain on even after the control signals have been removed. The lamps are turned off by opening the MOS which removes power to both the annunciator and the control and protection circuits. This also resets the SCR's by decreasing the anode-to-cathode current to zero.

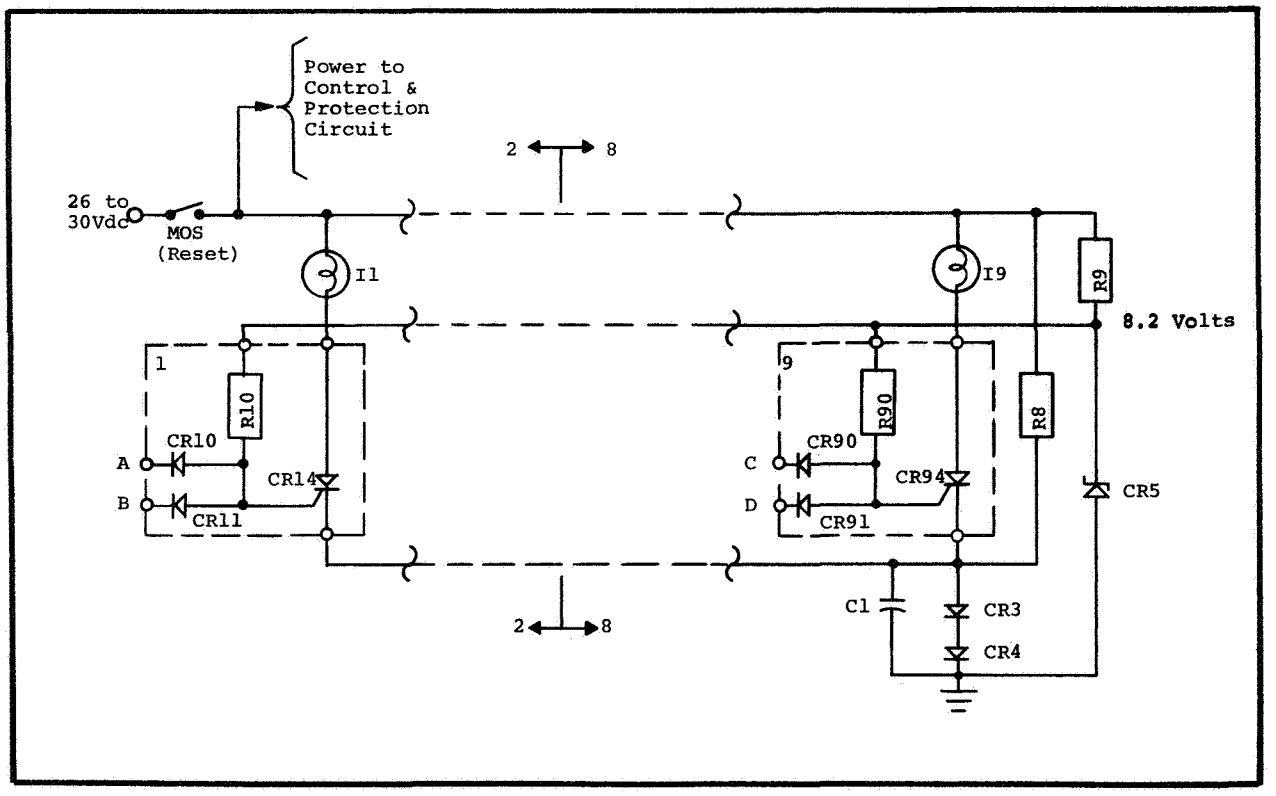


Figure 47. - SCR Lamp-Drive Circuit

Table VI. - Comparison of Lamp-Drive Circuits

Circuit	Total Components	Maximum Dissipation For Circuit at No-Fault Condition (watts)	Current to Control and Protection Circuit Transistors (ma)
SCR (figure 47)	51	0.2	0.130
2-Transistor (figure 48)	117	5.7	8.0
3-Transistor (figure 49)	144	5.4	0.150

Because the SCR's have a high current gain, the annunciator-control logic loads the respective transistors of the control and protection circuits at normally 130 microamperes. Resistor R9 and Zener diode CR5 provide a regulated 8.2-volt power supply for the SCR-gate drive resistors.

The power dissipation of the annunciator fault-indication circuit, at maximum input voltage, is 200 milliwatts. Each SCR lamp-drive circuit consists of four components. An additional six components are required which are common to all drive circuits. The total number of components for the fault-indication circuit is 51.

Two-transistor lamp-drive circuit. - Figure 48 shows the circuit required to operate the fault-indication lamps when the control is accomplished by transistors. The extra active device in this circuit is required to provide the latching function.

When no fault conditions exist, transistor Q11 is on, receiving its base drive through lamp I1. During this condition the current through lamp I1 is approximately one milliampere which is insufficient to light lamp I1. The maximum power dissipation, assuming a maximum input voltage of 30 volts, for each lamp-drive circuit at a no-fault condition is approximately 630 milliwatts; hence the entire fault-indication circuit requires about 5.7 watts. The required load on any one of the transistors in the control and protection circuits connected to pins A and B or C and D of figure 48 is normally eight milliamperes. Each transistor lamp-drive circuit consists of twelve components. The total number of components for the fault-indication circuit is 117.

Three-transistor lamp-drive circuit. - Figure 49 shows a second transistorized lamp-drive circuit. When no fault condition

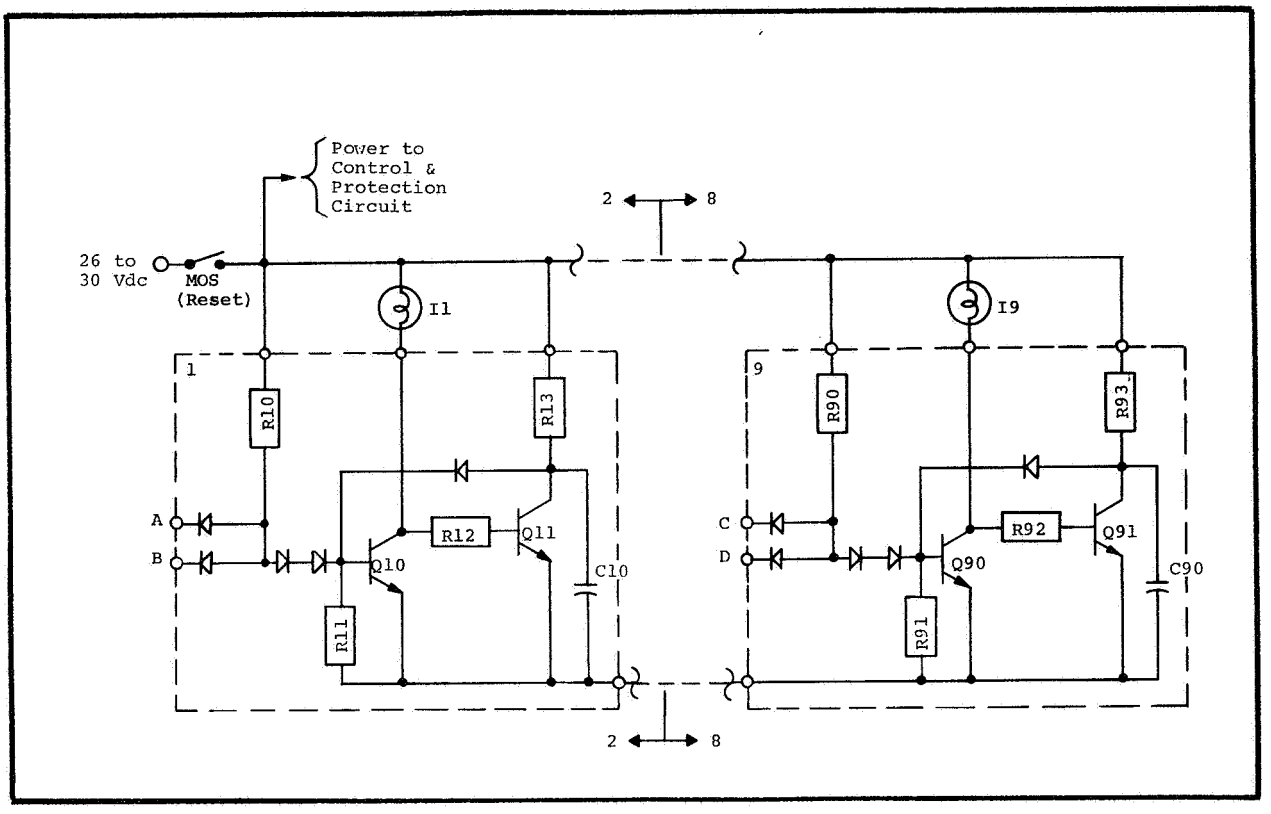


Figure 48. - Two Transistor Lamp-Drive Circuit

exists, transistor Q11 is on but no initial current is drawn through lamp I1. The maximum power dissipation for each lamp-drive circuit at a no-fault condition is approximately 600 milliwatts; thus the maximum dissipation for the fault-indication circuit is approximately 5.4 watts.

This method requires three more components per lamp-drive circuit than the previous approach, while wattage dissipation remains practically unchanged. The advantage of the three-transistor approach over the two-transistor approach is that the required load on any one of the transistors in the control and protection circuits connected to pins A and B or C and D is greatly reduced. The two-transistor circuit requires 8 milliamperes while the three-transistor circuit reduces the loading to 150 microamperes.

Multiple transistors are used to assure that once lamp I1 has been lighted it will remain lighted until the subsystem is reset. Each transistor lamp drive circuit consists of fifteen components. A total of 144 components is required for the fault-indication circuits.

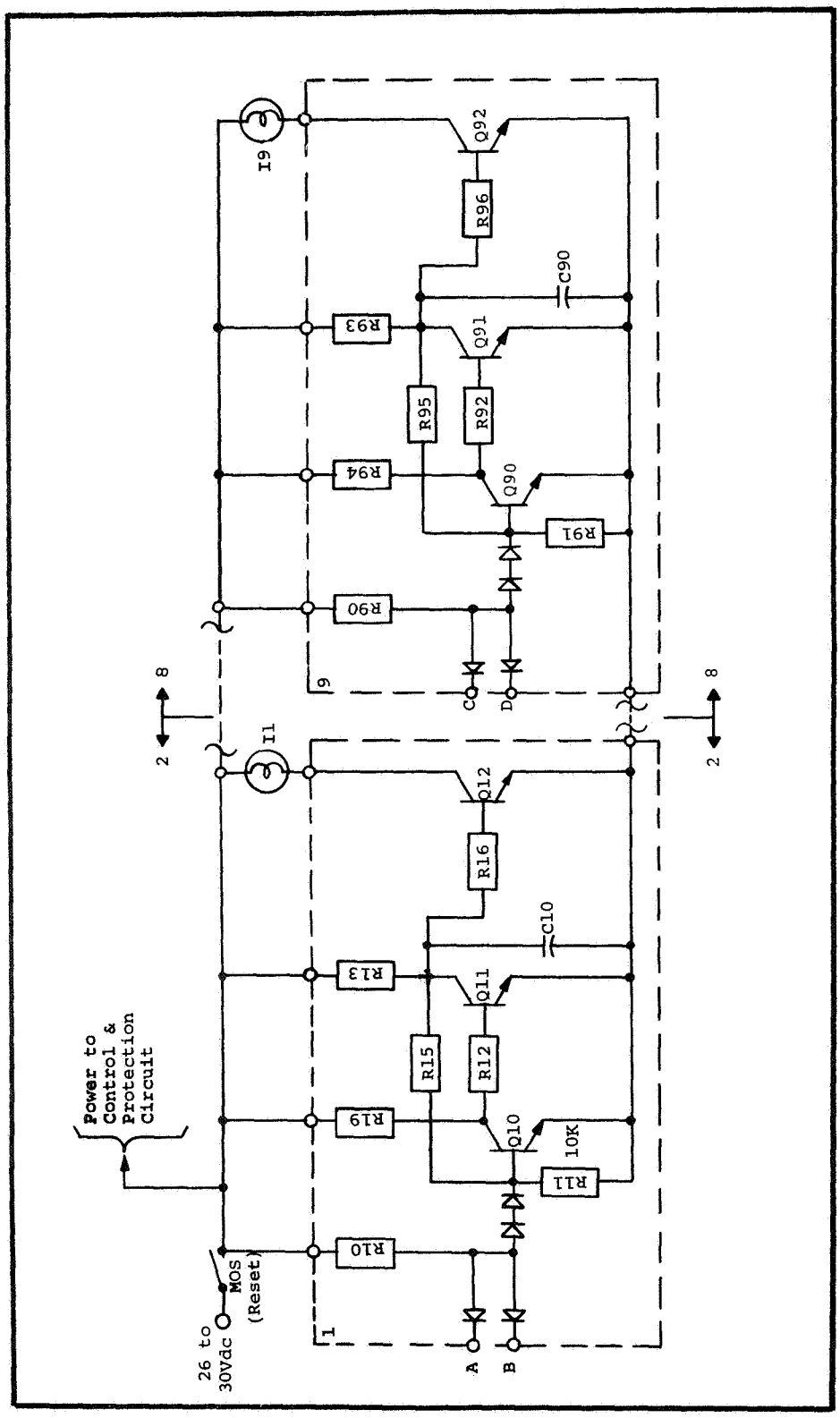


Figure 49. - Three Transistor Lamp-Drive Circuit

Annunciator Circuit Design

The complete annunciator circuit consists of lamps, lamp-drive circuits, signal amplifiers, an additional logic element, and a regulated voltage supply. The lamps are driven either by switches, auxiliary contacts of the contactors, or the SCR lamp-drive circuit. This section describes the lamp-drive circuit and the additional logic required to prevent multiple fault indications.

Fault-indication circuit. - Figure 47 shows a schematic diagram of the fault-indication circuit. The circuit consists of nine lamp-drive circuits identified as (I1 through I9). The SCR (CR14) controls the current through lamp I1. Once the SCR is turned on, it will remain on until the anode current is reduced to nearly zero. The AND gate consisting of diodes CR10 and CR11 and resistor R10 determines when CR14 will be turned on. The switch in series with the power supply (MOS) resets the control and protection circuits of the power subsystem. When MOS is in the reset position, power is removed from both the control and protection circuits and the annunciator. Thus, CR14 is turned off because no current flows from anode to cathode. Points A and B of the AND gate are connected to the collectors of transistors within the control and protection (C/P) circuits of either the inverter or the converter subsystem. Resistor R10 provides drive to the SCR gate whenever both diodes of the AND gate are reverse-biased. The gate current is supplied by an 8.2-volt regulated power supply consisting of resistor R9 and Zener diode CR5.

Additional annunciator fault logic. - The purpose of this logic is to prevent multiple-fault indications. Multiple faults are established when any fault shuts down an inverter or converter. Faults indicated when an inverter or converter is shut down are undervoltage and, for the inverter, underfrequency. Since the intent of the annunciator is to indicate only true faults, these multiple-fault indications must be prevented. Figure 50 shows the schematic diagram of figure 47 with the addition of a "lock-out" circuit.

The lock-out circuit is basically an AND gate with two stages of inversion. The input to the lock-out circuit is connected to the anodes of selected SCR's. If all the SCR's are off, the AND gate is satisfied (CR1, CR2, and CR3 reversed biased) and Q1 is off. If any one of the SCR's is on, Q1 is turned on, effectively grounding the gates of the SCR lamp-circuits through diodes CR4, CR5, and CR6.

The lock-out circuit then adds another condition to the AND gate of the fault-indicating circuit. For example, if signals X and Y represent two signals required to operate a fault indicator, the lock-out signal (LO) makes the conditions for lighting the lamp:

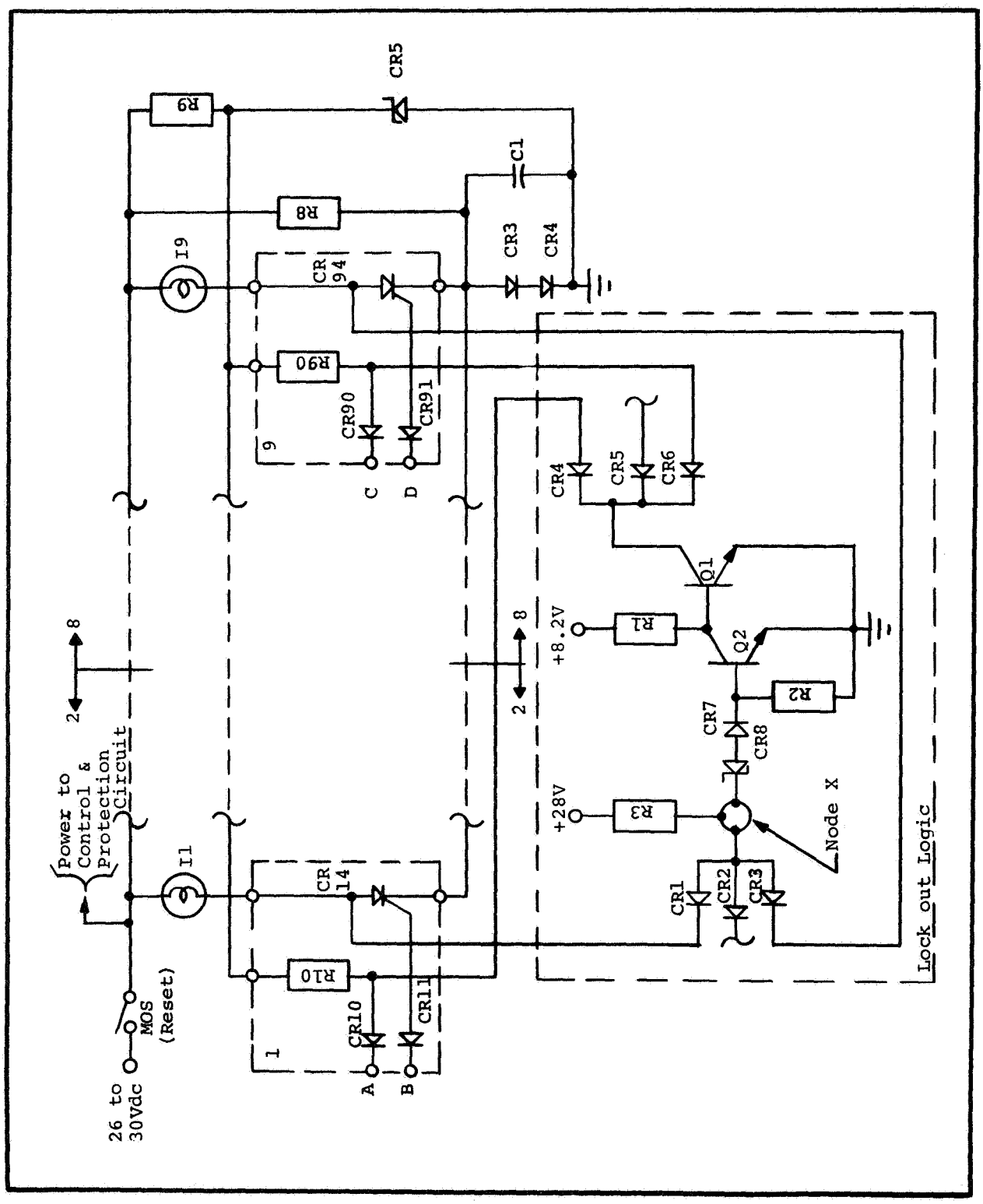


Figure 50. - Lamp-Drive Circuit with Lock Out Logic

$$\text{LIGHT LAMP} = X \cdot Y \cdot \overline{LO}.$$

This equation is read: the lamp is lighted only when signals X and Y and NOT LO are present.

Integration of annunciator with C/P logic circuit. - Signals from the control and protection logic circuits are defined in tables VII and VIII. These signals are applied to AND gates in the annunciator logic circuits to determine the appropriate lamp to light. The annunciator develops additional logic signals within itself to prevent multiple-fault indications. Multiple faults may be indicated when a system fault results in subsystem shutdown. The following faults cause either the ICC or CCC (figure 1) to trip: overvoltage (OV), undervoltage (UV), differential protection (DP), load bus (LB), overfrequency (OF), and underfrequency (UF). Lamps lit due to any of these signals activate the lock-out circuit previously described. The lock-out circuit prevents the OV, UV, UF, and OF lamps from lighting.

Table VII. - Required Logic Signals from Inverter Control and Protection Circuits to Operate Annunciator

Fault Condition (Lamp Identification)			Required Signals From Protection Logic
1	OV	(overvoltage)	A · E
2	UV	(undervoltage)	B · E
3	LD	(load division)	F
4	DP	(differential current)	G
5	LB	(load-bus overcurrent)	J
6	TB	(tie-bus overcurrent)	H · I
7	OF	(over frequency)	C · E
8	UF	(underfrequency)	D · E
9	FR	(frequency reference)	K

SIGNAL IDENTIFICATION	
A	Signal from OV sensing circuit
E	Signal from time delay activated by either OV, UV, OF, or UF sensing circuit
B	Signal from UV sensing circuit
F	Signal from LD sensing circuit and associated time delay
G	Signal from DP sensing circuit
J	Signal from load bus (LB) overcurrent sensing circuit and associated time delay
H	Signal indicating either a tie-bus or a load-bus overcurrent
I	Signal indicating that signal J is not present (NOT J)
C	Signal from OF sensing circuit
D	Signal from UF sensing circuit
K	Signal indicating failure in the reference frequency oscillator

Table VIII. - Required Logic Signals from Converter Control and Protection Circuits to Operate Annunciator

Fault Condition (Lamp Identification			Required Signals From Protection Logic
1	OV	(overvoltage)	A • C
2	UV	(undervoltage)	B • C
3	LD	(load division)	H
4	DP	(differential current)	E • F
5	LB	(load-bus overcurrent)	E • I
6	TB	(tie-bus overcurrent)	G • J

SIGNAL IDENTIFICATION

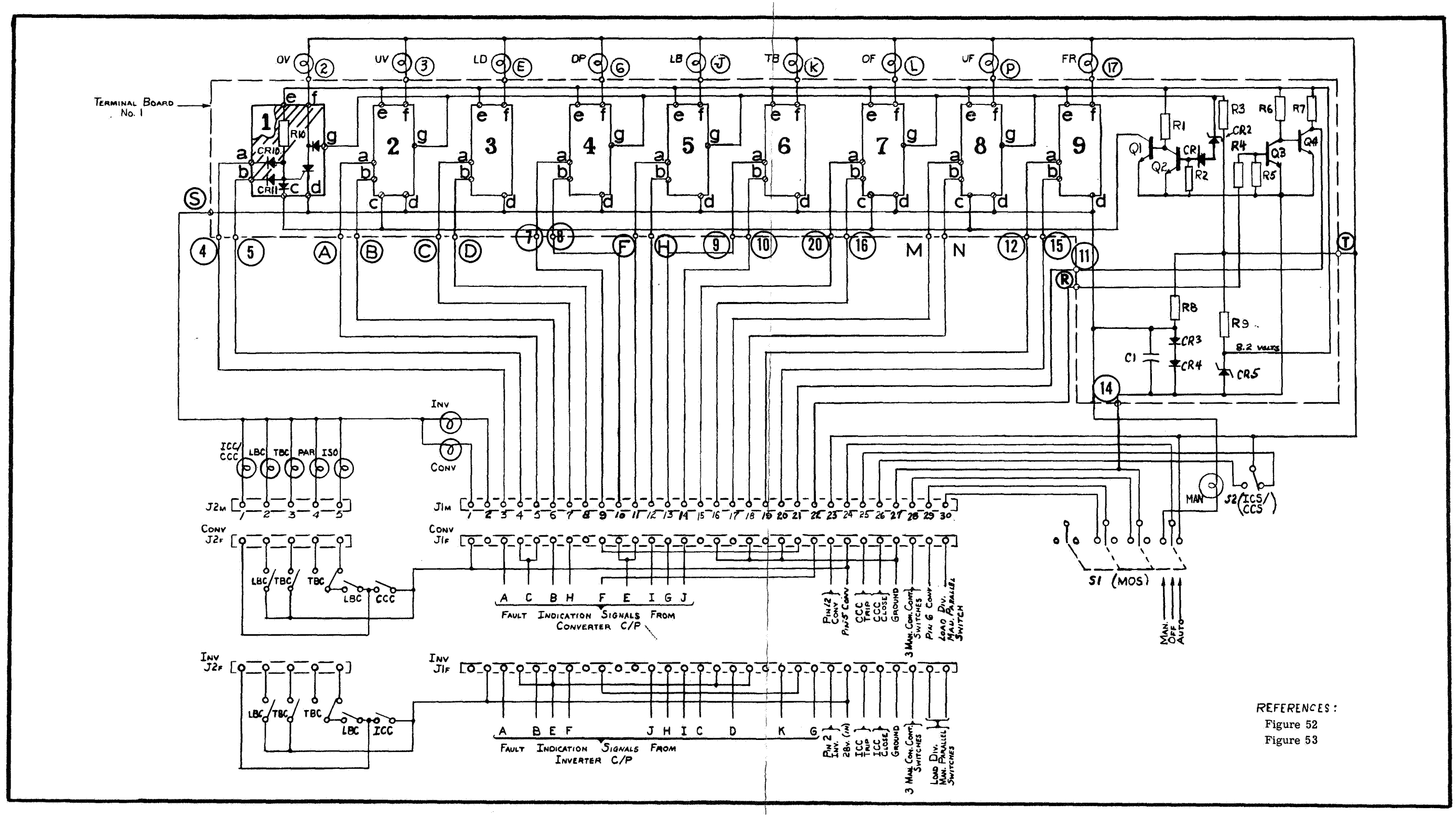
A	Signal from OV sensing circuit
B	Signal from UV sensing circuit
C	Signal from time delay activated by either OV or UV
H	Signal from LD sensing circuit and associated time delay
E	Signal representing either a DP or a Load-Bus Fault
F	Signal from DP sensing circuit
I	Signal indicating that a load bus overcurrent initiated signal E through time delays
G	Tie-bus contact or trip signal
J	Signal indicating that signal G was the result of a fault on the tie bus

Tables VII and VIII show the signal combinations for each fault indication. For example, the TB lamp is lit only when signals H (AND) I are present. The first of the two signals represent the sensed function, while the second indicates that a time delay has elapsed. This is necessary to prevent lamp lighting during transient abnormal conditions.

The AND gate drive for the SCR's represents a very small load on the protection circuits. Signal isolation is provided by the diodes in the AND gate. Hence, the operation of the protection circuits is not altered by the annunciator.

Annunciator Verification

Annunciator circuit design was verified by building two units for the control and protection circuits described in the report entitled "Inverter-Converter Automatic Paralleling and Protection" (ref. 2). Figure 51 is a schematic diagram of the annunciator circuit. Figures 52 and 53 show the origin of the signals in the inverter and converter control and protection cir-



REFERENCES:
Figure 52
Figure 53

Figure 51. - Annunciator System Schematic

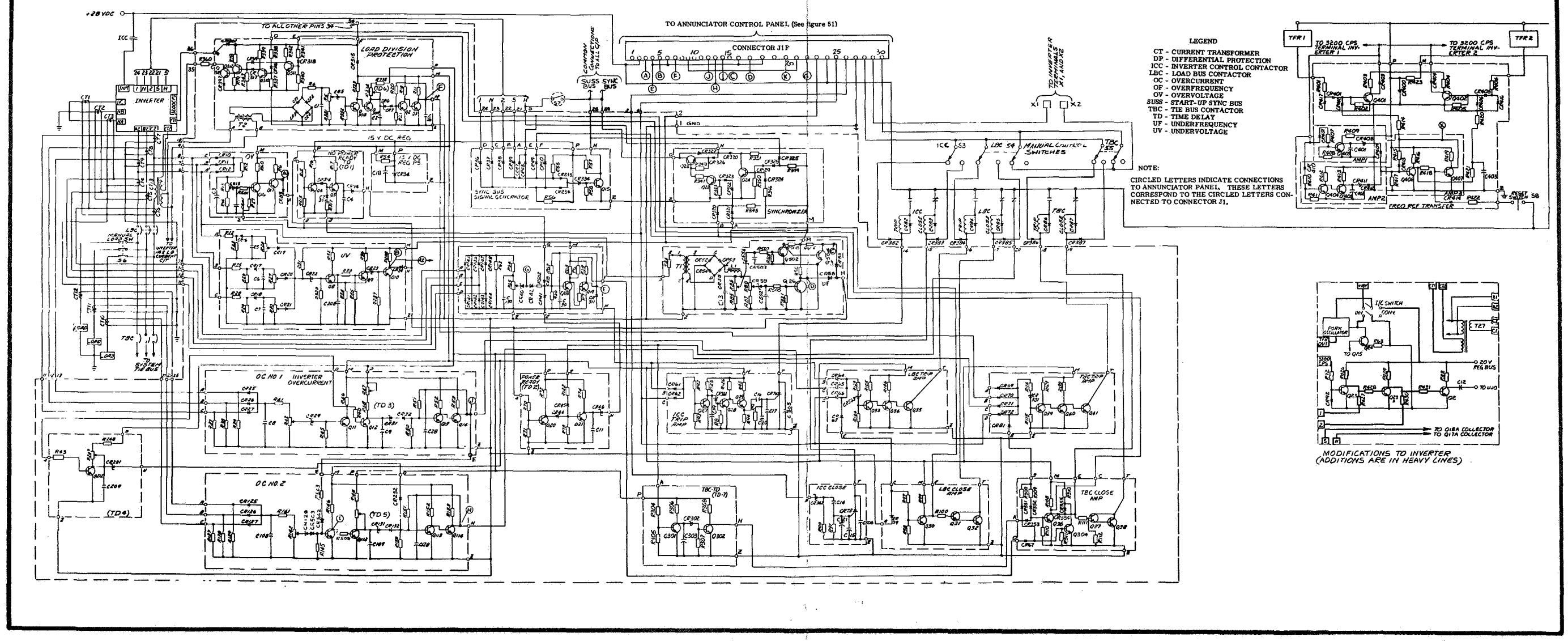
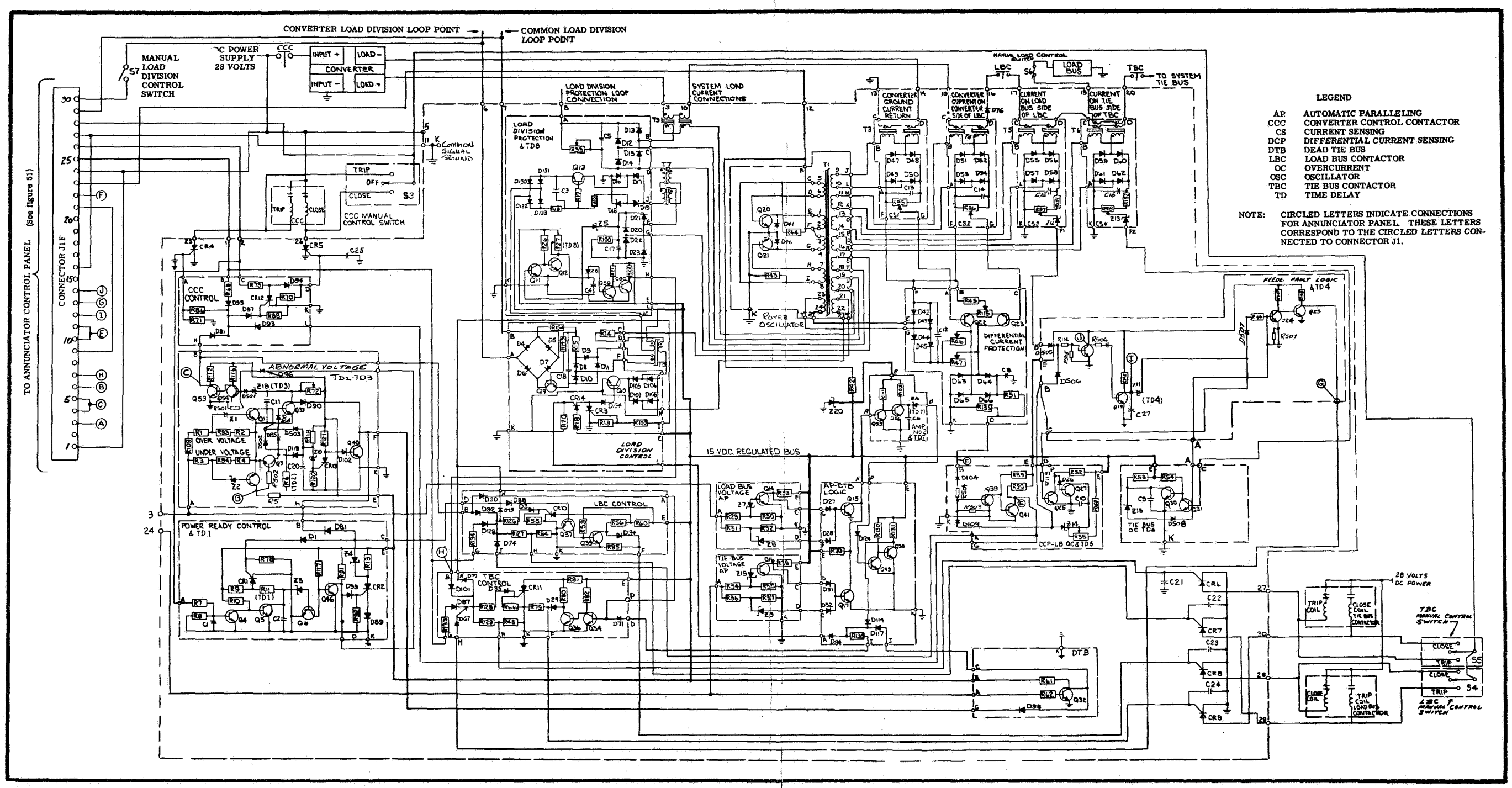


Figure 52. - Inverter Control and Protection Schematic



LEGEND

AP	AUTOMATIC PARALLELING
CCC	CONVERTER CONTROL CONTACTOR
CS	CURRENT SENSING
DCP	DIFFERENTIAL CURRENT SENSING
DTB	DEAD TIE BUS
LBC	LOAD BUS CONTACTOR
OC	OVERCURRENT
OSC	OSCILLATOR
TBC	TIE BUS CONTACTOR
TD	TIME DELAY

NOTE: CIRCLED LETTERS INDICATE CONNECTIONS FOR ANNUNCIATOR PANEL. THESE LETTERS CORRESPOND TO THE CIRCLED LETTERS CONNECTED TO CONNECTOR J1.

Figure 53. - Paralleled Converters Control and Protection Circuit Schematic

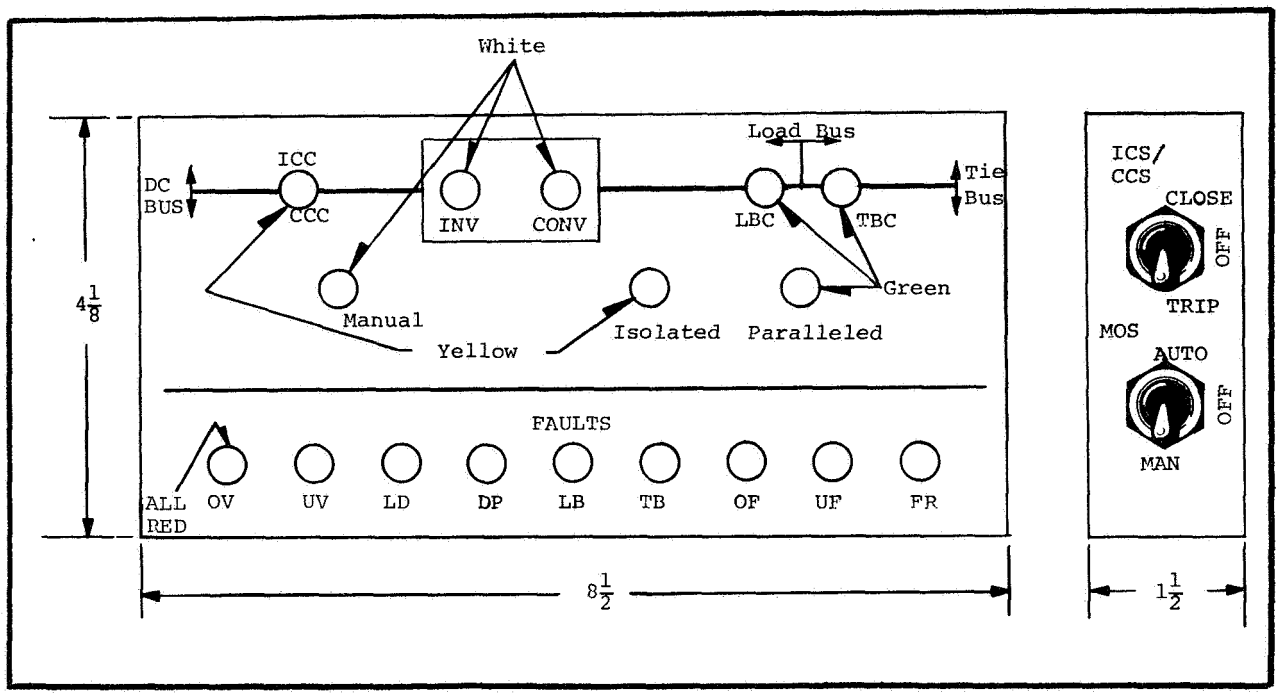


Figure 54. - Annunciator Front Panel

cuits used to operate the annunciator. Figure 54 shows the layout of the lamps and manual switches. The units were connected to both the paralleled ac and paralleled dc systems. The appropriate lamps were lit to indicate the various modes of system operation and the fault conditions applied to the system.

Annunciator Concluding Remarks

Design and experimental verification have demonstrated that a visual annunciator system can be used to display the state of an electric power system. This display indicates whether a multichannel electrical system is operating in a parallel mode or an isolated mode and also indicates whether an abnormal condition has occurred in the system.

Such an annunciation system can be used in either an ac or a dc system and requires a very small amount of power (e.g., 0.2 watts) from the system control and protection circuits.

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